Maximum Marks: 60
Credits: 04
Duration: Three Hours

Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.

Q.No. | Question | M.M.
--- | --- | ---
1(a) | Drive the input impedance of gm-C based temperature insensitive C-multiplier. Give the significance and applications of the circuit realized. | [08]
1(b) | In cascading the biquadratic filters how should the gain constant be selected to determine the signal level for each biquad? | [07]

2 (a) What are the effects of OTA non-idealities? | [05]
2 (b) Drive the input impedance of the active only ideal grounded inductor shown in Fig.1 Use this inductor for the realization of second order prototype band pass filter. Also give the expressions for filter parameters and calculate parameter sensitivities with respect to circuit. | [10]

![Active only grounded inductance simulator](image)

Fig. 1. Active only grounded inductance simulator

contd...
3(a) Define multioutput current controlled conveyor, give its symbol and characteristics equations.

3(b) Perform the analysis of current mode KHN filter using MOCCII. Give various filter parameters. Also give the translinear-C realization of KHN filter. Compare the two realizations.

4(a) Realize grounded and floating resistor using only CCCII.

4(b) Give the realization of universal cascadable current mode biquadratic filter using two CCCII and two grounded capacitors. Give various filter responses and filter parameters.

OR

5(a) What are the advantages and limitations of switched capacitor filters?

5(b) Describe the implementation of a MOS double polysilicon capacitor and its parasitic. How these parasitic are made ineffective in building blocks?
2013-14
M.TECH. (WINTER SEMESTER) EXAMINATION
ELECTRONICS ENGG.
CURRENT MODE CIRCUITS AND APPLICATIONS
EL-618

Maximum Marks: 60  Credits: 04  Duration: Three Hours

Answer any FIVE questions.
Assume suitable data if missing.
Notations used have their usual meaning.

Q.No.  Question                                                                                                           M.M.
1  Explain the non-interactive cascading requirements in the four basic amplifier topologies. Realize each of the four
    topologies with known devices/building blocks.  [12]
2(a)  Justify the superiority of voltage amplifiers built using CFOA over the ones built using VOA.  [08]
2(b)  Design a current-mode lossy integrator circuit using a single CCII and perform the parasitic analysis of the circuit.
                          [04]
3  Analyze the circuit of Figure 1 and comment on the function performed; derive the relationship between various output
    currents. Also analyze the circuit using non-ideal model of CCCIIs with parasitic considerations.  [12]

[Diagram]

Fig. 1
4. "AD844 is a versatile IC for realizing current-mode circuits". Justify the statement with at least six suitable examples.

5. Design current conveyor based circuits to perform the functions: (i) sine to square wave conversion, (ii) square to triangular wave conversion, (iii) triangular to square wave conversion, (iv) squarer.

6(a). Distinguish clearly between the BJT and CMOS Translinear loops. Design a voltage follower using each.

6(b). Find the transfer function(s) of the circuit shown in Fig. 2 and discuss the function performed.

![Fig. 2](image)

7(a). Explain the design and working of a current-mode Algorithmic ADC.

7(b). Analyze the quadrature oscillator circuit of Fig. 3, so as to find the frequency and condition of oscillation, assuming ideal CDBAs.

![Fig. 3](image)
2013-14
M.TECH. (WINTER SEMESTER) EXAMINATION
ADVANCE MICROPROCESSOR SYSTEM & DESIGN
EL-641

Maximum Marks: 60 Credits: 04 Duration: Three Hours

Answer all the questions. Assume suitable data if missing. Notations used have their usual meaning.

Q.No. Question M.M.
1(a) What do you mean by microcontroller? Mention few applications of microcontrollers. [05]
1(b) Give a brief account of comparison between various family members of 8051. [07]

OR

1(b)' Compare and contrast between 8048 and 8051 microcontrollers. [07]

2(a) What are the salient features of INTEL's-8086 microprocessor? Explain with an example how 20 bit physical address is calculated?. [07]

2(b) What is an interrupt? Explain hardware and software interrupt of 8086. [05]

OR

2(b)' Write an 8086 assembly language program to find out the largest number from an array of 16-bit numbers stored in a memory location starting at address 0800H in the segment 1000H. [05]

3(a) Explain features and architecture of 8087. [07]

3(b) Describe with examples the data types available in 8087. Give the range of values that can be represented by these data type. [05]

OR

3(b)' Describe the interfacing of 8087 coprocessor with 8086 microprocessor. [05]
4(a) Write short notes on any one of the following.
   (i) 80286
   (ii) 80386

4(b) Explain the necessity of decoding when memory device is attached to a microprocessor? A 64K ROM is to be interfaced with 8086 processor. Two 32K x 8 chips are available. Perform memory mapping from address F0000H.

5(a) Draw the architecture of Pentium processor and explain the features of Pentium processor.

OR

5(b) Illustrate dual processors and a hyper-threaded processor with diagrams. Also explain different versions of multi core technology processors.
### Question Details

<table>
<thead>
<tr>
<th>Q.No.</th>
<th>Question</th>
<th>M.M.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1(a)</td>
<td>With regard to format of baseband signals for data transmission, describe the advantages of bipolar signaling over unipolar and polar types of signalling. Is there any disadvantage of bipolar signaling compared to unipolar and polar types of signaling.</td>
<td>[5]</td>
</tr>
<tr>
<td>1(b)</td>
<td>In the context of digital data transmission, what are (i) isolated errors, (ii) burst errors. Also, give examples of practical situations where each of these types of errors are caused.</td>
<td>[5]</td>
</tr>
<tr>
<td>1(c)</td>
<td>What are the examples of biphase schemes, in general? Give examples of practical communication systems / networks where the biphase schemes are actually used.</td>
<td>[5]</td>
</tr>
<tr>
<td>2(a)</td>
<td>Illustrate that all the biphase schemes other than the Manchester format are differential schemes.</td>
<td>[5]</td>
</tr>
<tr>
<td>2(b)</td>
<td>Explain the advantage(s) offered by duobinary and modified duobinary waveforms.</td>
<td>[5]</td>
</tr>
<tr>
<td>2(c)</td>
<td>Explain very briefly how the effect of ISI can be minimized by proper timing of the pulse train and sampling intervals as they relate to system bandwidth.</td>
<td>[5]</td>
</tr>
<tr>
<td>3(a)</td>
<td>Give a brief account of Nyquist’s vestigial symmetry theorem.</td>
<td>[5]</td>
</tr>
<tr>
<td>3(b)</td>
<td>The sampled impulse response of a baseband channel is given by ( V = [1 \ 0.4] ). (i) Design a single tap linear feedback transversal equalizer for the given channel. (ii) Find the impulse response of the channel and the equalizer taken together.</td>
<td>[5]</td>
</tr>
<tr>
<td>3(c)</td>
<td>Discuss why the equalizers should be ‘adaptive’ for use in mobile radio environments.</td>
<td>[5]</td>
</tr>
</tbody>
</table>

*contd...*
4(a) With regard to time varying channels, explain in detail the working of a receiver using combined detector and estimator in a wireless system.

4(b) How can catastrophic failure occur in a receiver employing a combined detector and estimator? How can a receiver avoid such a failure or recover from it quickly?

5(a) Give a brief description of classification of modems.

5(b) With the help of a suitable diagram, explain the connection set-up, two-way alternate data transfer, and connection clearing sequences of RS/EIA-232C/D interface.

5(c) What are the limitations of RS-232 interface standard? Suggest a way in which some improvement can be obtained.

6 Write short notes on any THREE of the following:
   (i) Performance of Linear and Non-linear Equalizers
   (ii) Maximum Likelihood Sequence Estimation
   (iii) “Intelligent operations” of a modem
   (iv) Bluetooth Radio (RF) layer
   (v) Inquiry and paging in a Bluetooth network
2013-14
M.TECH. (WINTER SEMESTER) EXAMINATION
ELECTRONICS ENGINEERING
WIRELESS COMMUNICATION
EL-658

Maximum Marks: 60    Credits: 04    Duration: Three Hours

Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.

Q. No.                        Question                                           M. M

1(a) In a mobile system, channel estimation is performed every 4.615 ms. If the carrier frequency [04]
is 900 MHz, determine the mobile velocity for which system will work satisfactorily.

1(b) Show that a two-path channel with maximum delay spread very large compared to symbol [05]
duration introduces frequency selective fading.

1(c) Prove that a Rayleigh fading signal has an exponential pdf for the instantaneous SNR. [06]

OR

1(c') Determine the probability of occurrence of a deep fade in Rayleigh fading channel. Discuss [6]
how this relates to the average bit error rate (BER) in Rayleigh fading channel.

2(a) Determine the necessary SNR, in order to detect BPSK signal with an average BER of $10^{-5}$ [04]
for a Rayleigh fading channel.

2(b) Consider an M-branch receiver diversity system where each branch receives an independent [05]
Rayleigh fading signal. Drive an expression for the average SNR at the output when the
combiner uses equal weight for all the M received signals.

OR

2(b') Consider a single branch Rayleigh fading signal has a 20% chance of being 6 dB below some [05]
mean SNR threshold. Determine the mean of the Rayleigh fading signal as referenced to the
threshold. Also, find the likelihood that a three branch selection diversity receiver will
operate 6 dB below the mean SNR threshold.

2(c). Consider a wireless system with two-antenna transmit diversity is employing Alamouti's scheme. Show how to recover the transmitted symbols and achieve dual diversity reception.

3(a). Consider a flat-fading channel of bandwidth 20 MHz where for a fixed transmit power $S$, the received SNR is one of four values: $\gamma_1 = 30$ dB, $\gamma_2 = 20$ dB, $\gamma_3 = 10$ dB and $\gamma_4 = 0$ dB. The probability associated with each state is $p_1 = 0.2$, $p_2 = 0.3$, $p_3 = 0.3$ and $p_4 = 0.2$. Assume both transmitter and receiver have CSI. Find the optimal power allocation policy for this channel and its corresponding Shannon capacity. Compare this capacity with the channel capacity in AWGN with the same average SNR.

4(b). Discuss how OFDM converts a frequency selective channel into a set of parallel narrowband channels.

4(c). Consider an OFDM system having 256 subcarriers with subcarrier bandwidth of 15.625 kHz. Compute the OFDM symbol duration and the transmission bandwidth of the system.

4(d). Consider an OFDM system with symbol duration 64 $\mu$s and cyclic prefix (CP) period is 12.5% of the symbol duration. Compute the loss in spectral efficiency due to CP.

OR

4'(a) Discuss briefly the principle of SC-FDMA. What advantages does it offers for the reverse link (MS to BS) of a mobile system.

4'(b) Discuss how a MIMO system can be used to provide multiplexing gain.
MTech Electronics Engg(Examination)

C & I System

Advanced Digital Signal Processing EL -661

MM=60 Time- 3 Hour

Attempt any Four Questions.
Assume suitable data if missing any.

Q1 Design a one stage and two stage Interpolator to meet the following specifications.
I=20 , Input sampling rate = 10000Hz, Pass band 0<F<90, transition band 90<F<100
Ripple \( \delta_t = 10^{-2} \), \( \delta_w = 10^{-3} \) (15)

Q2(a) Write the input output relation ship for a decimation process of a factor five. (8)
Q2(b) Explain the polyphase decomposition process. (7)

Q3(a) Determine the power spectra for the random process generated by the difference equation
\[ X(n) = -0.81X(n-2) + w(n-1) \]
Where \( w(n) \) is a white noise process with variance \( \sigma^2 \). (10)

Q3(b) Briefly discuss the various non parametric methods of power spectrum estimation. (5)

Q4 Consider a wide sense stationary process \( u(n) \) whose autocorrelation function has the following values for different lag
\[ r(0) = 1, \ r(1) = 0.8, \ r(2) = 0.6, \ r(3) = 0.4 \]
a, use the Levinson -Durbin recursion to evaluate the reflection coefficient \( k_1, k_2, k_3 \).
b, set up a three - stage lattice predictor for this process. (15)

Q5, Consider a wiener filtering problem characterized as follows: The correlation matrix \( R \) is given as
\[
R = \begin{bmatrix}
1 & 0.5 \\
0.5 & 1
\end{bmatrix}
\]
The cross correlation vector \( P \) between input and desired response is
\[
P = \begin{bmatrix}
0.5 \\
0.25
\end{bmatrix}^T
\]
Evaluate the tap weights of the Wiener filter and minimum mean square error produced by this filter. (15)

Q6, Develop the complex canonic form of lattice predictors. Draw the block diagram and flow graph and explain the operation. (15)
2013-14
M. TECH. (WINTER SEMESTER) EXAMINATION
ELECTRONICS ENGINEERING
MICROWAVE DEVICES & INTEGRATED CIRCUITS
EL-673

Maximum Marks: 60
Credits: 04
Duration: Three Hours

Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.

<table>
<thead>
<tr>
<th>Q.No.</th>
<th>Question</th>
<th>M.M.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1(a)</td>
<td>Why scattering (S) parameters are used for characterization of microwave devices? Calculate the S-parameters of a shunt element (Y) shown in Fig. 1</td>
<td>[05]</td>
</tr>
<tr>
<td>1(b)</td>
<td>What are the various device technologies available to implement wireless transceiver circuits? Which one do you think gives a cost effective solution? Explain.</td>
<td>[05]</td>
</tr>
<tr>
<td>1(c)</td>
<td>2G and 3G communications are centered around 900MHz and 2GHz bands, respectively. Compare these bands in terms of quality of service and coverage area.</td>
<td>[05]</td>
</tr>
</tbody>
</table>

**OR**

| 1'(a) | Explain the term 'Beyond 3G'. Make a comparison among 2G, 3G and 4G wireless systems on the basis of quality of service, roaming and types of switching.                                              | [05] |
| 1'(b) | Is it possible to scale-down Si MOSFETs to nano-scale range? Explain how scaling improves transit-time frequency $f_t$.                                                                                       | [05] |
| 1'(c) | Assume that the GaAs device used in the design of power amplifier (PA) is replaced by Si MOSFET. Explain what effect it has on PA performances.                                                               | [05] |

*contd ... 2*
2(a) Explain why in wireless circuit design impedance is usually maintained at 50Ω. Use a simplified model of MOSFET to determine input impedance $Z_{IN}$ of circuit shown in Fig. 2.

![Fig. 2](image)

<table>
<thead>
<tr>
<th>2(b)</th>
<th>What do you mean by 'Channel Length Modulation' used in short channel MOSFETs? Explain its effect on output impedance.</th>
</tr>
</thead>
<tbody>
<tr>
<td>2(c)</td>
<td>Make a comparison between 40GHz and 60 GHz wireless PANs. Suggest suitable device technology for their design.</td>
</tr>
</tbody>
</table>

**OR**

<table>
<thead>
<tr>
<th>2'(a)</th>
<th>What is a low noise amplifier? Make use of appropriate analytical expression to explain that it is the crucial block of the receiver shown in Fig. 3.</th>
</tr>
</thead>
</table>
| 2'(b) | Explain the following terms used in design of rf circuits:  
   i) Linearity  
   ii) Power added efficiency (PAE) |
| 2'(c) | What are the essential differences in a low frequency (<1GHz) and microwave (>1GHz) transistors? Why microwave transistors are designed using multi-fingers? |

<p>| 3(a) | Give design flow of radio frequency circuits and briefly explain the various steps involved. |
| 3(b) | Give the physical origin parasitic resistances $R_{SB}$, $R_{DSB}$ and $R_{DB}$ used in the model shown in Fig. 4. Carry out y-parameter analysis of the model to show that |</p>
<table>
<thead>
<tr>
<th>4(a)</th>
<th>Differentiate between the power match and the noise match. Why do you think they are not possible to achieve simultaneously in radio frequency circuit design.</th>
<th>[05]</th>
</tr>
</thead>
<tbody>
<tr>
<td>4(b)</td>
<td>A shielded strip-line has the following parameters: dielectric constant of the insulator $\varepsilon_{rd} = 2.56$; strip width $w = 0.7\text{ mm}$; strip thickness $t = 1.4\text{ mm}$; shield depth $d = 3.5\text{ mm}$. Determine (i) the fringe capacitance (ii) the characteristic impedance.</td>
<td>[05]</td>
</tr>
<tr>
<td>4(c)</td>
<td>How the effect of gate and source terminals parasitics are modeled at radio frequency (&gt;1GHz)? Explain.</td>
<td>[05]</td>
</tr>
</tbody>
</table>
M.TECH. II\textsuperscript{nd} (WINTER SEMESTER) EXAMINATION
ELECTRONIC CIRCUITS AND SYSTEMS DESIGN
LOW POWER VLSI DESIGN
EL-727

Maximum Marks: 60 Credits: 04 Duration: Three Hours

Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.

Q.No. Question

1(a). Explain with the help of a timing diagram how parallelism can be used to achieve low power instead of high performance in realizing digital circuits. [04]

1(b). What is glitching power dissipation? How can it be minimized? [04]

1(c). Explain voltage scaling using High-Level Transformations. [04]

OR

1(a\textsuperscript{'}). Determine the short circuit power dissipation of static CMOS inverter shown in Fig. 1. Explain the effect of large and small load capacitance on short circuit current. [06]

\begin{center}
\includegraphics[width=0.3\textwidth]{fig1.png}
\end{center}

\textbf{Fig. 1}

1(b\textsuperscript{'}). Consider a correlator example in which the correlation length is 1024; the sample whose values range from \(-7\) to \(+7\) are accumulated at 64MHz, a 4-bit random number is transferred to an accumulator register at 64MHz. Explain and show how the architecture of accumulator and transition activity is varied in two’s complement and sign magnitude representation. [06]
2(a). Explain differential codebook tree structure vector quantization techniques for minimizing switched capacitance.

2(b). Explain how Differential Current Switch Logic (DCSL) with precharged high reduces internal voltage swing.

2(e). Explain how One Hot Coding and Bus Inversion Coding help in reducing the switching activity.

3(a). Explain any two low voltage design techniques to minimize leakage in standby mode.
   i. Transistor stacking
   ii. Multithreshold CMOS (MTCMOS)
   iii. Double gate dynamic threshold SOI (DGDT-SOI)

3(b). List the hierarchy of limits of low power design. Explain any one of them.

4. Distinguish between conventional charging used in static CMOS circuit and adiabatic charging of a load capacitance? Explain how dynamic power dissipation is minimized using adiabatic switching. Explain the read operation in adiabatic SRAM core.

5(a). Explain read and write Static Noise Margin (SNM) in a 6T SRAM cell.

5(b). Explain Instruction Level Power Analysis (ILPA) approach for software power estimation.

OR

5(a)'. Explain how banked organization of SRAM and divided word line architecture helps in reducing power in SRAM.

5(a)''. Discuss software power optimization technique using minimizing memory access cost.

*******************************************************************************