1. (a) What do you understand by Cascade Realization?
   (b) Determine the optimal ordering out of the \((n/2)!\) possibilities in which the biquads can be connected to form the cascade network, also give the possible ways to cascade the biquads for \(6^{th}\) order network.

   **OR**

1'. Discuss comprehensively, similarities, differences, advantages, drawbacks between
   (i) Op amp-RC filters  (ii) OTA-C filters  (iii) Translinear-C filters and
   (iv) SC-filters.

2. (a) What are the effect of OTA nonidealities?
   (b) Give the \(gm-C\) realization of ideal grounded integrators and differentiators using OTA and grounded capacitors. Also give attractive features of the circuits.

   **OR**

2'. (a) What are the specific features of current mode filters?
   (b) Give the realization of cascadable current mode second order bandpass filter using two OTAs and two grounded capacitors. Find the sensitivities of filter parameters to the passive elements. Also give some attractive features for the circuit.

3. (a) What are the effects of nonidealities of the current conveyors or the frequency performance of the circuits?
   (b) How can we realize (i) voltage follower and (ii) current follower using a CCCII.
   (c) Give the parasitic insensitive switched capacitor realization of positive and negative resistors.

4. (a) What is the desirable input and output impedance for an active current mode filter? Justify your answer.
   (b) Give the translinear-C realization of ideal grounded inductor and ideal floating inductor. Use the ideal grounded inductor for the realization of monolithic biquadratic filters.
2011-2012
M. TECH (II SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
CURRENT MODE CIRCUITS AND APPLICATIONS
(EL-618)

Maximum Marks: 60

Duration: Three Hours

NOTE: (i) Answer all questions.
(ii) Assume suitable data if necessary.
"Students governed by the old ordinance will be examined out of 75 marks and their obtained marks shall be proportionately raised."

1. (a) Discuss the problems associated with voltage-mode circuits, which led to the popularity of current-mode circuits. (4)

1 (b) What are the desirable characteristics of a current-mode circuit? (4)

1 (c) Analyze the circuit of Figure 1 for I_{out} and explain the circuit’s function. (4)

2 (a) "CFOA based voltage amplifier exhibits a bandwidth independent of closed loop gain". Justify the statement. (7)

2 (b) How can we realize a DX-CCII using four AD-844 ICs? (5)

3 (a) Explain the function of the circuit as shown in Figure 2. How do parasitic capacitances influence the circuit function? (5)

3 (b) Suggest a possible implementation of a bit cell of a current-mode algorithmic ADC. Explain its advantages, limitations, and ways to overcome the limitations. (7)

4 Figure 3 shows a DVCC-based quadrature oscillator circuit; analyze the same for its characteristic equation, frequency of oscillation and condition of oscillation. Suggest suitable means to make the circuit electronically tunable. Now, considering parasitics as: R_x=100\Omega, C_y=C_z=0.2\text{pF}, find the error introduced in the frequency of oscillation and the error in quadrature relation between v_1 and v_2.

OR

4’ Synthesize the block diagram of Figure 4 using CCCIIIs and capacitors, such that each block operates in current-mode. Also explain the function performed, both qualitatively as well as quantitatively. (12)

Contd...
5 Write detailed technical notes on any

(a) Field Programmable Analog Arrays
(b) CCCII based four quadrant Analog Multipliers
(c) Current-mode DACs
(d) Current-mode precision rectifiers
(e) CCII – based Instrumentation amplifiers
Note: (i) “Students governed by the old ordinance will be examined out of 75 marks and their obtained marks shall be proportionately raised.”
(ii) Answer any FIVE questions.

1. (a) Give typical SRAM’s basic organization schematic and storage cell array. Describe Read and Write operation of six transistor CMOS SRAM cell. (06)
(b) A typical double-polysilicon technology CMOS-SRAM process is to be converted to high performance BiCMOS memory system, explain the process in detail. (04)

2. (a) Discuss working of an emitter coupled logic (ECL) memory RAM cell. (04)
(b) Sketch and explain a stacked CMOS-SRAM cell schematic cross-section. (04)
(c) Discuss briefly serially accessed memories. (04)

3. (a) Sketch cross-section of a planar DRAM cell and discuss how storage charge capacity can be increased. Also mention basic requirements of a good cell. (7.5)
(b) Sketch a typical 1Mb DRAM using trench capacitor and describe the use of inputs RAS and CAS strobes. (4.5)

4. (a) Describe substrate-plate-trench (SPT) memory cells and discuss the need to go for inverted trench cells. (06)
(b) Define ‘soft error’ and ‘soft error rate’ and discuss some methods to reduce the susceptibility to soft errors. (06)

5. (a) Describe ULSI DRAM development in 64-256 Mb range and technology challenges faced during this development stage. (06)
(b) Sketch either NOR or NAND ROM array and describe its working and discuss relative merits and demerits. (06)

6. (a) Give an schematic of 4 bits in a stacked fuse array. What are its two main features? (03)
(b) Sketch stacked-gate EPROM transistor, equivalent circuit and describe operation of floating-gate EPROM cell. (05)
(c) Describe a LAP cell and advance processes and technologies involved in it. (04)

7. (a) Discuss briefly MNOS and SONOS memories. (05)
(b) Give equivalent circuit and cross-section of textured-polysilicon EEPROM. (02)
(c) Discuss non-volatile SRAM. (05)
M.TECH. WINTER (II SEMESTER) EXAMINATION
(ELECTRONICS CIRCUIT & DESIGN/COMMUNICATION AND INFORMATION SYSTEMS)
ADVANCED MICROPROCESSOR SYSTEM & DESIGNING
(EL-641)

Max Marks : 60

Duration : Three Hours

Note: (i) “Students governed by the old ordinance will be examined out of 75 marks and their obtained marks shall be proportionately raised.”
(ii) Answer all questions.

1. (a) What is a microcontroller? Also explain what are essential sections of microcontroller.

(b) Describe the internal block diagram of 8051 microcontroller.

07

(b’) Explain 8048 signals.

OR

08

2. (a) Explain the following pins of 8086:

(a) NMI (b) BHE (c) TEST (d) LOCK

OR

07

(a’) Explain Flag register of 8086.

(b) Determine the effect of each one of the following 8086 instructions:

(i) PUSH [BX] ii) DIV DH

(iii) CWD iv) MOVSB v) MOV START [BX], AL

Assume the following data prior to execution of each one of the instruction independently.

[DS] = 3000H [AX] = 0049H

[ES] = 5000H [SI] = 0400H

[DX] = 0400H [DI] = 0500H

[SP] = 5000H DF = 0

[SS] = 6000H [BX] = 6000H

[36000H] = 02H [36001 H] = 03H

[50500H] = 05H [30400H] = 02H

[30401H] = 03H

08

3. (a) Explain features and architecture of 8087 arithmetic coprocessor.

OR

07

(a’) Explain the function and format of 8087 status register. Also list the status bits and their applications.

Contd.....2,
2.

(b) What are the different data types handled by the coprocessor?

(c) What is DDR memory?

4. (a) What is hyper-threading technology? How does hyper-threading technology work?

OR

(a') Compare the Pentium with the Pentium PRO microprocessors.

(b) How many general purpose registers are available in the Pentium?

(c) Describe the 80386 memory system and explain the purpose and operation of the bank selection signals.
II Semester M.Tech. Examination (Electronics Engg.)
(Communication & Information Systems)

EL- 652 Data Transmission Systems

Maximum Marks: 60 Time: 3 hours

"Students governed by the old ordinance will be examined out of 75 marks and their obtained marks shall be proportionately raised".

Any missing data can be suitably assumed.
Symbols used have their standard meanings. Answer any FOUR questions.

1 (a) It is often said that bipolar NRZ signaling for baseband data transmission has an inherent but small amount of error detection capability. Why? (5)

(b) NRZ-M uses an ex-OR gate while NRZ-S uses an ex-NOR gate in the encoder. Would the NRZ-M encoder output be an inverted form of NRZ-S encoder output, for the same input data sequence? Give justification for your answer. (5)

(c) Give your comments on the synchronization capability of (i) duobinary waveform, (ii) modified duobinary waveform. (5)

2 (a) Taking help of binary transmission as an example, explain the advantage/disadvantage of differential encoding in case (i) isolated errors, (ii) burst errors. (10)

(b) Discuss the advantages and limitations of bi-phase techniques, in general. (5)

3 (a) Explain very briefly how the effect of ISI can be minimized by proper timing of the pulse train and sampling intervals as they relate to system bandwidth. (5)

(b) Show that raised cosine spectrum is a special case of sinusoidal roll-off spectrum. (5)

(c) The sampled impulse response of a baseband channel is given by $V = [1 \ \frac{1}{2}]$. (5)
(i) Design a single tap linear feedback transversal equalizer for the given channel.
(ii) Find the impulse response of the channel and the equalizer taken together.

4 (a) A wireless system is such that the various multi-path components (corresponding to the instantaneous value of the transmitted signal) always reach the receiver terminal at the same time instant. How much will be the time delay spread in this case? Is equalization required in this case? (5)

(b) With regard to time varying channels, explain the working of a receiver using combined detector and estimator. (10)

contd... 2
5 (a) Give a brief description of classification of modems. (5)

(b) With the help of a suitable diagram, explain the connection set-up, two-way alternate data transfer, and connection clearing sequences of RS/EIA-232D interface. (5)

(c) Distinguish between multi-level TDM, multiple-slot TDM, and pulse-stuffed TDM. (5)

6. Write short notes on any THREE of the following: (15)
   (i) Maximum Likelihood Sequence Estimation
   (ii) Similarities and differences between Bluetooth and Zigbee
   (iii) CDMA2000 / EVDO / 3G
   (iv) MIMO / WIMAX
   (v) Internet Telephony
2011-12
M. TECH. Winter (II Semester) Examination
ELECTRONICS ENGINEERING
(Communication and Information Systems)
EL-653 (Voice and Picture Coding)

Max. Marks: 60
Duration: 03 Hours

Notes:

(i) Attempt any FIVE questions.
(ii) Symbols have their usual meanings.
(iii) Assume any suitable data, if needed.

1. (a) With the help of suitable diagrams, discuss the anatomy and physiology of human visual system.

   Consider that the vocal tract of a person is modeled as an open ended cylindrical tube and is of length 16 cm. For a glottis pulse as an excitation signal, find the first three formant frequencies of the generated sound wave.

   Differentiate between temporal and frequency masking in human hearing system. Explain the various frequency masking parameters, and elaborate relationship among them with the help of suitable diagram.

2. (a) What is the tri-receptor theory? With the help of chromaticity diagram, explain the color perception of human visual system.

   With the help of suitable diagrams, state and explain 2-D sampling theorem for images. What are the effects of under sampling in images? Explain.

   Show that to quantize a signal having uniform probability distribution function, the optimal quantizer is a uniform quantizer.

3. (a) Prove the following statistical properties of a Max-Lloyd quantizer;
   (i) Quantizer output is an unbiased estimate of input.
   (ii) The quantization error is uncorrelated with quantized output.
   (iii) The variance of quantizer output is reduced by a factor (1-D(n)), where D(n) is the mean square distortion of n-bit quantizer for unity variance input.

   Consider a speech signal x(t) having probability density function close...
to Laplacian function defined as, \( p(x) = \frac{1}{\sqrt{2\pi} \sigma_x} e^{-\frac{1}{2} |x|/\sigma_x} \). Design an four level (L=4) optimal quantizer for this speech signal, assuming unity variance of signal \( x(t) \), (i.e. \( \sigma_x^2 = 1 \)).

4. (a) Draw the block diagram of a logarithmic quantizer and show that the signal to noise ratio (SNR) is independent of signal variance and depends only upon the step size.

(b) For speech signal, generally an adaptive quantizer is preferred over an optimal quantizer. Why? Consider a feedback adaptive quantization system shown in Fig. 1 (a). The two bit quantization characteristic and codeword assignment is shown in Fig. 1(b). Suppose the step-size is adapted according to the following rule:

\[ \Delta(n) = M \Delta(n-1) \]

Where \( M \) is a function of previous codeword \( c(n-1) \) and \( \Delta_{\text{min}} \leq \Delta(n) \leq \Delta_{\text{max}} \). Further suppose that \( M = \begin{cases} P & \text{if } c(n-1) = 01 \text{ or } 11 \\ \frac{1}{P} & \text{if } c(n-1) = 00 \text{ or } 10 \end{cases} \)

Draw the block diagram of step adaptation system.

5. (a) Derive the conditions for perfect reconstruction in two-band subband coding, ignoring the effect of quantization error.

(b) Derive the relationship between Discrete cosine transform (DCT) and discrete Fourier transforms (DFT) and show that DCT is not the real part of DFT.

(c) Name the transforms having following properties:
   (i) Rectangular basis function
(ii) Optimal transform
(iii) Easier to implement
(iv) Sawtooth function as basis function
(v) Energy compaction property close to the optimal transform
(vi) Signal dependent basis function

(d) Why short-time Fourier transform (STFT) is not suitable for non-stationary signals?

6. (a) Consider a 4x4 image, whose wavelet transformed coefficients (with one stage of 2-D DWT) are given in Fig. 2.

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This image is coded using SPIHT algorithm. Find the bits generated by the encoder in the first two-passes (two most significant bit-planes). Using these bits, find the reconstructed wavelet coefficients at the decoder.

(b) Describe some of the salient features of JPEG2000 coder, which makes it different from JPEG coder.

(c) Explain the concept of quality and resolution scalabilities in modern image coders. Also, discuss the means to achieve SNR scalability.

7. (a) Most of the video coders use hybrid structure. Why? Name the computationally most expansive operation in a video coder.

(b) With the help of suitable example, explain full search block-based motion estimation and compensation. Which criterion is used to find near optimal motion vectors?

(c) With reference to H.264/AVC coder, explain the following in brief:
   (i) Intra prediction
   (ii) Variable block motion estimation/compensation
   (iii) Switching frames
MTech Electronics Engg(Examination) 2011-2012
(C & I System)
Advanced Digital Signal Processing EL-661

MM=60

Time- 3 Hour

Attempt any Four Questions. Assume suitable data if missing any.

Q1 Design a one stage and two stage Interpolator to meet the following specifications.(15)

I=20, Input sampling rate = 10000Hz, Pass band 0≤F≤90, transition band 90≤F≤100

Ripple: \( \delta_1 = 10^{-2} \), \( \delta_2 = 10^{-3} \)

Q2(a) Show that the transposition of an L stage interpolator for increasing the sampling rate by an integer factor I

is equal to an L stage decimator that decreases the sampling rate by a factor D = I.(10)

Q2(b) Discuss the multi resolution property of wavelet transform.(5)

Q3(a) Determine the power spectra for the random process generated by the difference equation

\[ x(n) = 0.81x(n-2) + w(n-1) \]

Where w(n) is a white noise process with variance \( \sigma_w^2 \).(10)

Q3(b) Briefly discuss the various non parametric methods of power spectrum estimation.(5)

Q4 A signal \( x(n) = s(n) + w(n) \) is given where s(n) is an AR process that satisfy the difference equation,

\[ s(n) = 0.6s(n-1) + v(n) \]

Where v(n) is a white noise sequence with variance \( \sigma_v^2 = 0.64 \) and w(n) is a white noise sequence with variance \( \sigma_w^2 = 1 \). Design a wiener filter of length M=2 to estimate s(n). Also determine the corresponding minimum MSE.(15)

Q5(a) An AR process is defined by the difference equation.

\[ x(n) = x(n-1) - 0.6x(n-2) + w(n) \]

Where w(n) is a white noise process with variance \( \sigma_w^2 \). Use the Yule Walker equation to solve for values of the auto-covariance.(10)

Q5(b) Briefly discuss the recursive least square method.(5)

Q6 Develop the complex canonic form of lattice predictors. Draw the block diagram and flow graph and discuss the operation.(15)
2011-2012

M. TECH WINTER (II SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
(COMMUNICATION AND INFORMATION SYSTEM)
MICROWAVE DEVICES & ICs
(EL-673)

Maximum Marks: 60          Duration: Three Hours

"Students governed by the old ordinance will be examined out of 75 marks and their obtained marks shall be proportionately raised".

Note: Attempt Any Four questions
Assume suitable data if required any
Terms used have their usual meanings.

1 (a) What do you mean by S-parameters? For the given 3-port circulatory device (See Fig. 1), the power fed at port 1 is collected at next port i.e. at port 2. Similarly, power fed at port 2 is collected at port 3 and so on. Assume that each port is perfectly matched; calculate S-matrix of the device.

![Diagram of 3-port device]

Fig. 1

1(b) What do you mean by "Channel Length Modulation" used in short channel MOS devices? Explain how it affects the output impedance of the rf devices.

1(c) Explain the term "Beyond 3G". Make a comparison among 2G, 3G and 4G wireless systems on the basis of quality of service, roaming and types of switching.

2(a) i) Assume that the MOS device used in the design of low noise amplifier (LNA) is replaced by HEMT. Explain what effect it has on LNA performances.

ii) Why common gate (CG) configuration is less noisy than common source (CS)? Explain.

Contd...
2(b) Differentiate between heterodyne and homodyne radio transceivers. Given Fig. 2 and Fig. 3, which one do you think is a better choice for heterodyne transceiver?

![Diagram of heterodyne and homodyne transceivers](image)

2(c) What is a low noise amplifier (LNA). Make use of appropriate analytical expression to explain that "LNA" is the crucial block of the receiver shown in Fig. 4.

![Diagram of receiver block diagram](image)

3(a) Is it possible to scale-down multiple gates MOSFETs to nano-scale range (<100nm). Explain how scaling improves transit-time frequency, $f_T$ of such devices.

3(b) Write short notes on modeling of the following parasitic elements:
   (i) Gate resistance
   (ii) Source resistance

4(a) Explain why in wireless circuit design impedance is usually maintained at 50Ω. Use a simplified model of MOSFET to determine input impedance $Z_{IN}$ of circuit shown in Fig. 5.

![Diagram of MOSFET model circuit](image)

4(b) i) It has been found that analog circuits at rf (>1GHz) do strange things. Explain.
   ii) Discuss briefly the various steps involved in the design of class-E power amplifier.

Concl. ...
4(c) What are the various front-end blocks used in latest wireless communication system? Briefly discuss their design goals and objectives.

5(a) What is transit frequency $f_T$? Show that for short-channel MOSFET $f_T$ is given as

$$f_T \approx \frac{v_{sat}}{2\pi L}$$

Where $v_{sat}$ = saturation velocity; $L$ = gate length.

5(b) Give physical origin of each model component shown in Fig. 6. Carry out $y$-parameters analysis of the model to show that

$$C_M + C_{GD} = -\frac{Im(Y_{21})}{\omega} - g_m R_G (C_{GS} + C_{GD})$$

![Fig. 6]

6(a) What are the advantages of monolithic microwave integrated circuits (MMIC) over discrete circuits? List the basic characteristics required for an ideal substrate.

6(b) With help of suitable diagram explain the working of micro-strip lines. Briefly discuss their advantages with respect strip-lines as well as coaxial lines.