2010 – 2011
M.TECH. (II SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
CURRENT MODE CIRCUITS AND APPLICATION
(EL – 618)

Maximum Marks : 75

Note: Answer all questions.
Answer parts of one question together.
Make suitable assumptions (if needed)

1. (a) Discuss the realization of following using current mode active building blocks. [10]
   (i) Differential-input differential-output voltage to current converter.
   (ii) Differential-input current follower.
   (iii) Differential-input current to voltage converter.
   (iv) Differential-input voltage follower.
   (v) Biphase voltage follower.

(b) With the help of suitable example(s) discuss the advantages of current-mode circuits. [5]

2. (a) Derive the adjoint circuit for the oscillator as shown in Figure 1. [6]
    (b) Transform the voltage-mode circuit of Figure 2 into current-mode circuit using only three CCII's. [6]
    (c) Convert the opamp based voltage-mode circuit of Figure 2 into a cell based voltage mode equivalent. [3]

3. Quantitatively compare the (i) gain-bandwidth product and (ii) slew rate of voltage opamp with current feedback opamp. [15]

OR

3'. Explain the realization of any six current-mode active elements using AD-844's. [15]

4. (a) Obtain a relation between the marked currents (I₁, I₂, I₃ and I₄) in Figure 3. [4]
    (b) Explain the principle of operation of current-scaling DAC. Show the realization of a 4-bit CCCII-based DAC. [7]
    (c) Explain the operation of a current-mode Sample-Hole circuit. [4]

OR

4'. Using the parasitic model of CCCII, analyze the circuit of Figure 4 for its CMRR. [15]

5. (a) Analyze the circuit of Figure 1 using the parasitic model of CCII. Discuss the circuits performance deviations from the ideal behaviour. [7]
    (b) Explain the function performed by the circuit of Figure 5. Analyze and relate I₁ and I₂. Modify the circuit to sense I₁, I₂ and their phase-inverted versions all at high output impedance. [8]

Contd.....2
Maximum Marks: 75
Duration: Three Hours

Note: Answer all questions. Make suitable assumptions wherever necessary.

1(a) Sketch Vout vs Vin in Fig. 1 as Vin varies from 0 to 3V. (5)

1'(a) Sketch Vout vs Vin in Fig. 2 as Vin varies from 0 to 3V. (5)

1(b) Sketch the capacitances $C_{EM}$ and $C_{EF}$ of the transistor shown in Fig. 3 as $V_x$ moves from 0 to 4V. Assume $V_{TH}=0.5V$. (5)

1(c) Explain the subthreshold region of operation of a MOS transistor. (5)

2(a) Assuming all MOSFETs are in saturation, calculate the small-signal voltage gain of the circuit shown in Fig. 4. (5)

2'(a) Assuming all MOSFETs are in saturation, calculate the small-signal voltage gain of the circuit shown in Fig. 5. (5)

2(b) The cascode of Fig. 6 is designed to provide an output swing of 1.9V with a bias current of 0.5mA. If $\gamma=0$ and $(W/L)_{T1} = W/L$, calculate $V_{b1}$, $V_{b2}$ and W/L. What is the voltage gain if L=0.5um. (10)

2'(b) A differential pair uses input NMOS devices with W/L=50/0.5 and a tail current of 1mA. Assume $V_{DD}=3V$, $\mu_nCox=60\mu A/V^2$, $\mu_pCox=30\mu A/V^2$, $\gamma = 0$, $V_{THN}=|V_{THP}|=0.7V$, $\lambda_n=0.1V^{-1}$, $\lambda_p=0.2 V^{-1}$ for a channel length of 0.5um.

(i) What is the equilibrium overdrive voltage of each transistor?
(ii) How is the tail current shared between the two sides if $V_{in1}-V_{in2}=50mV$?
(iii) What is the equivalent $G_m$ under this condition? (4+3+3)

3(a) Calculate the differential voltage gain if $I_{ss}=1mA$, $V_{(W/L)_{T1,2}}=50/0.5$ and $(W/L)_{T3,4}=50/1.0$ for the circuit shown in Fig. 7. What is the minimum allowable input CM level if $I_{ss}$ requires at least 0.4V across it? Using this value of $V_{in,CM}$, calculate the maximum output swing. Assume $V_{DD}=3V$ and device data given in question 2'(b). (3+3+3)
3(b) Determine the CMRR of a differential amplifier shown in Fig. 8 with \((W/L)_{t,g}=50/0.5\) and \(I_D=0.5\text{mA}.\)

(6)

4(a) Calculate the gain at very low and very high frequencies for the circuit shown in Fig. 9. Neglect all other capacitances and assume \(\lambda=0.\)

(10)

4(b) Calculate the input impedance of the circuit shown in Fig. 10.

(5)

4'(b) Calculate the input referred thermal noise voltage of circuit shown in Fig. 11.

(5)

5(a) What is the need of compensation in CMOS OPAMP? Explain briefly the techniques used for compensating a CMOS OPAMP.

(5)

5(b) Design the opamp shown in Fig. 12 for the following requirements: maximum differential swing=4V, power dissipation=6mW, \(I_{ss}=0.5\text{mA}\) with a supply voltage of 3V. Assume device data given in 2'(b).

(10)

OR

5'(b) Design a folded cascade OPAMP shown in Fig. 13 to satisfy the following specifications: \(V_{DD}=3\text{V}\), Differential output swing=3V, power dissipation=10mW, voltage gain=2000. Use device parameters given in question 2'(b).

(10)

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Figures attached

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2010-2011
II SEMESTER M.TECH. EXAMINATION:
ELECTRONICS ENGINEERING
IC PROCESSES AND FABRICATION
EL-623

Max. Marks: 75

Time: Three Hours

Attempt ANY FIVE Questions

1 a Briefly describe the specifications, installations, operations and automation of clean rooms.

1 b Describe either the zone refining or the Czochralski crystallisation process for producing single crystal silicon suitable for microelectronic production.

2 a What is catastrophic failure? What is RCA clean? What is supercritical fluid cleaning?

2 b Differentiate between wet cleaning and dry cleaning? Explain in detail wet cleaning process.

2 c What is the need of Si epitaxy? Describe the process of vapor phase epitaxy.

3 a Briefly describe the advantages and disadvantages of APCVD. How PECVD is different from LPCVD?

3 b Assume that the gas AB is introduced into a reactor and that the only chemical reaction that occurs in the chamber is

\[ AB \longleftrightarrow A + B \]

If the process is run at 1 atm (760 torr) and temperature of 1000 K the process reaches chemical equilibrium, calculate the partial pressure of each species. The equilibrium constant for the reaction is given by

\[ K_p(T) = 1.6 \times 10^9 \text{torr} e^{\frac{-2.94T}{kT}}. \]

4 a If LPCVD polisilicon deposition has an activation energy of 1.65 eV and a deposition rate of 8 nm/min at 600 C, what is the deposition rate at 620 C?

4 b What are the advantages of Molecular Beam Epitaxy (MBE). With the help of sketch, explain the operation of MBE system.
4 c What are the advantages and disadvantages of PVDs? With the help of sketch, explain the operation of a typical vacuum evaporation system.

5 a What are the useful properties of silicon dioxide? Describe the process of thermal oxidation. Differentiate between dry oxidation and wet oxidation. How the thickness of oxide is related with the thickness of consumed silicon?

5 b Describe the photolithography process step by step with the help of sketches. What is the difference between isotropic and anisotropic etching?

5 c How the isolation is achieved in Integrated circuit fabrication among the devices? Describe the various techniques.

6 a With the help of sketch, explain the operation of a typical ion implantation system.

6 b Draw the circuit diagram of simple 2 input TTL NAND gate. With the help of sketches, explain the all fabrication steps of simple 2 input TTL NAND gate.

7 With the help of sketches, explain the all fabrication steps of BiCMOS integration process by taking a simple circuit.
2010-2011
M.TECH. (II SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
SEMI-CONDUCTOR MEMORIES
(EL-633)

Maximum Marks: 75
Duration: Three Hours

Answer any five questions.

1. (a) What are the advantages of SOI technology? Describe a most commonly used SOI technique including its specific advantages and limitations. 06
(b) Discuss 16-64 Mb SRAM development. 09

2. (a) Describe the working of a dual port RAM and sketch its basic logic circuit. 07
(b) Describe Read, Programming and Erase Operation of an ETOX cell. 08

3. Describe in detail, construction and working of a MOS SRAM cell and its peripheral circuits. 15

4. (a) Sketch schematic x-section of a planar DRAM cell, discuss signal charge and how it can be increased. Why the planar cell was not practically used beyond 1 Mb density? 11
(b) What is the basic criterion for DRAM cell design especially beyond 1 Mb density level? 04

5. (a) Discuss briefly:
   (i) EDO DRAM
   (ii) EDRAM and
   (iii) HSDRAM. 7½
(b) Sketch schematic and explain a non-volatile SRAM cell. 7½

6. (a) Discuss open bit line and folded bit line architecture in DRAMs. 4½
(b) Give advantages of half-V<sub>cc</sub> bit line sensing in CMOS DRAMs. 4½
(c) Sketch basic one transistor storage cell structure with cross-coupled latch sense amplifier. Why a dummy cell was used in it? 06

7. (a) Describe a floating--gate EPROM cell in detail. 07
(b) Describe SPEAR and LAP cells for realizing EPROMs. 08
2010 – 2011
M.TECH (II SEMESTER) EXAMINATION
(ELECTRONIC CIRCUIT & DESIGN/COMMUNICATION AND INFORMATION SYSTEMS)
ADVANCED MICROPROCESSOR SYSTEM & DESIGN
(EL-641)

Maximum Marks: 75

Note: Answer all questions.

1. (a) What are the minimum structural units and devices needed in a microcontroller? (03)
   (b) What are the different ways of classifying the types of the microcontroller? (04)
   (c) Explain the 8048 pins/signals (08)

   OR
   (c') Draw the architecture of 8051 MCU. (08)

2. (a) Give the internal architecture of 8086 microprocessor. Also explain the
     function of its each unit. (07)

   OR
   (a') Write 8086 assembly program to compute \( \sum_{i=1}^{N} X_i Y_i \) where \( X_i \) and \( Y_i \) are signed
     8-bit numbers. \( N = 100 \). Assume CS and DS are already initialized. Assume no
     overflow. (07)
   (b) Explain how the address space is physically implemented in 8086 uP. Also
     explain the process of even-addressed word transfer and odd-addressed word
     transfer. (08)

3. (a) Draw the internal structure of the 80 x 87 arithmetic coprocessor and explain
     the functions of its major sections. (08)

   OR
   (a') Explain the function and format of 80 x 87 status register. Also list the status
     bits and their applications. (08)
   (b) What is the size of the stack in the 8087?
   (c) Which are the different data types handled by the coprocessor? (03)
   (d) What is the difference between a “processor” and an “interfacing chip”. (02)

4. (a) Describe common address-decoding techniques, as well as the decoders that
     are found in many systems. (10)

   OR
   (a') Develop a 32-bit-wide memory interface that contains EPROM memory at
     location FFFFF000H – FFFFFFFFH. (10)
   (b) What are the different types of ROM available? (05)

5. (a) How many address lines are found in the Pentium Pro system. (02)

   OR
   (a') In what way is Pentium Pro an improvement over Pentium. (02)
   (b) How many caches are found in the Pentium and what are their sizes? (05)
   (c) How much memory can be addressed by the Pentium II? (03)
   (d) What is a core 2 processor? (05)

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NOTE: (i) Answer any FIVE questions.
(ii) Any missing data can be suitably assumed.
(iii) Symbols used have their standard meanings.

1 (a) With regard to format of baseband signals for data transmission, describe the advantages of bipolar signaling over unipolar and polar types of signalling. Is there any disadvantage of bipolar signaling compared to unipolar and polar types of signalling. (5)

(b) NRZ-M uses an ex-OR gate while NRZ-S uses an ex-NOR gate in the encoder. Would the NRZ-M encoder output be an inverted form of NRZ-S encoder output, for the same input data sequence? Give justification for your answer. (5)

(c) What are the advantages of biphase signaling schemes, in general? Give at least one example of its use in a system standard. (5)

2 (a) Give your comments on the synchronization capability of (i) duobinary waveform, (ii) modified duobinary waveform. (5)

(b) Describe briefly the Miller (Delay Modulation) waveform. (5)

(c) Explain very briefly how the effect of ISI can be minimized by proper timing of the pulse train and sampling intervals as they relate to system bandwidth. (5)

3 (a) A computer outputs binary symbols at a rate of 56 kbit/s. Find the baseband bandwidths required for each of the following roll-off factors if sinusoidal roll-off spectral shaping is used: $\alpha = f_s/f_c = 0.25, 0.5, 0.75, \text{ and } 1.0$. (5)

(b) The sample at time instant $t = iT$ of a digital baseband received signal is given by:

$$r_i = s_i + 2.5 s_{i-1} + s_{i-2} + w_i.$$ Determine the tap gains of the 11-tap linear feedforward transversal equalizer for the given channel. (10)
4 (a) The sampled impulse response of a baseband channel is given by $V = [1 \quad \frac{1}{2}]$. 
(i) Design a single tap linear feedback transversal equalizer for the given channel.
(ii) Find the impulse response of the channel and the equalizer taken together.

(b) Discuss why the equalizers should be ‘adaptive’ for use in mobile radio environments.

5 (a) Give a brief description of classification of modems.

(b) What is meant by “intelligent operations” of a modem? Which interchange circuits of RS / EIA-232D are used for this?

(c) What are the limitations of RS-232 interface standard?

6 (a) Distinguish between multi-level TDM, multiple-slot TDM, and pulse-stuffed TDM.

(b) What is balanced signalling and what is its advantage? Give examples of interface standards that use this method.

(c) Describe briefly the role of training signals in data transmission systems.

7 Write short notes on any THREE of the following:
(i) Nyquist’s Vestigial Symmetry Theorem
(ii) Maximum Likelihood Detection
(iii) V.32 and V.32bis dial-up modems
(iv) OFDM and its use in DSL modems
(v) Use of cable TV network for data transmission & internet access.
1. (a) Explain the relations and/or dependence between delay spread, mobile velocity, coherence bandwidth and coherence time.

OR

(a') Suppose we have an application that requires a power outage probability of 0.01 for the threshold $P_0 = -80$ dBm. For Rayleigh fading, what value of the average signal power is required?

(b) Consider a wideband channel characterized by the autocorrelation function

$$A_c(\tau, \Delta t) = \begin{cases} \sin c(w\Delta t) & 0 \leq \tau \leq 10 \mu sec \\ 0 & \text{else} \end{cases}$$

where $w = 100$ Hz.

i. Does this channel correspond to an indoor channel or an outdoor channel, and why?

ii. Compute the channel’s average delay spread, rms delay spread, and Doppler spread.

iii. Over approximately what range of data rates will a signal transmitted over this channel exhibit frequency selective fading?

iv. Assuming that the channel exhibits Rayleigh fading, what is the average length of time that the signal power is continuously below its average value?

2. (a) For a Rayleigh fading channel, determine the required average signal-to-noise-ratio (SNR) for a given minimum SNR $\gamma_0$ and outage probability $P_{out}$.

(b) Drive an expression for the distribution of received SNR, if the envelope of the received signal is Rayleigh distributed.

OR

(b') Consider a wireless communication system employing M-branch receiver diversity with selection combining. Drive an expression for the outage probability at the combiner output.
3. (a). Consider a wireless communication system in which channel side information (CSI) is known at both transmitter and receiver. Specify an optimum power allocation strategy to maximize the channel capacity.

(b). Consider a flat-fading channel where for a fixed transmit power $S$, the received SNR is one of four values: $\gamma_1 = 30$ dB, $\gamma_2 = 20$ dB, $\gamma_3 = 10$ dB, and $\gamma_4 = 0$ dB. The probability associated with each state is $p_1 = .2$, $p_2 = .3$, $p_3 = .3$, and $p_4 = .2$. Assume both transmitter and receiver has CSI. Find the optimal power control policy $S(i)/S$ for this channel and its corresponding Shannon capacity per unit Hertz.

OR

(b'). Consider a time-invariant frequency-selective block fading channel consisting of three subchannels of bandwidth $B = 1$ MHz. The frequency response associated with each channel is $H_1 = 1$, $H_2 = 2$ and $H_3 = 3$. The transmit power constraint is $P = 10$ mW and the noise PSD is $N_0 = 10^{-9}$ W/Hz. Find the Shannon capacity of this channel and the optimal power allocation that achieves this capacity.

4. (a). Find the equivalent parallel channel model for a MIMO channel with channel gain matrix

$$H = \begin{bmatrix} .1 & .3 & .7 \\ .5 & .4 & .1 \\ .2 & .6 & .8 \end{bmatrix}$$

(b). Drive an expression for the capacity of a static MIMO channel.

OR

(b'). Calculate the capacity of a MIMO system when CSI is unknown at the transmitter.

5. (a). Describe briefly how OFDM works. What are the key advantages of OFDM over single carrier systems, such as WCDMA?

(b). A list of parameters of an OFDM system is given as follows: 64 subcarriers (48 for data, 4 for pilots and 12 null subcarriers), symbol duration is 4µs, 0.8µs for cyclic prefix, and system bandwidth is 20MHz. Calculate the FFT time-period, sampling frequency, number of samples in the guard interval and subcarrier frequency spacing.

OR

(b'). Demonstrate mathematically, the multipath rejection capability of a direct sequence spread spectrum (DSSS) system.
2010-2011
M.TECH. (II SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
(COMMUNICATION AND INFORMATION SYSTEM)
SECURE COMMUNICATION
(EL-657)

Maximum Marks: 75

Duration: Three Hours

Do all the five questions.
Assume suitable values of data, if not given.

1.(a) Make a suitable table to determine the values of \( a^b \mod n \) for:
   (i) \( a = 11, n = 93 \) and \( b = 11, 23, 46 \) and \( 92. \)
   (ii) \( a = 23, n = 31 \) and \( b = 5, 11, 23 \) and \( 47. \)

1'(a) Consider the finite field \( \mathbb{GF}(2^3) \) defined over the irreducible polynomial \( (x^3 + x^2 + 1) \)
and show that \( g^5 + g + 1, g^8 = g, g^{10} = g^2 + 1, g^k = g^{k \mod 7}. \)

1'b) Consider \( \mathbb{GF}(2^5) \) defined over the irreducible polynomial \( m(x) = x^8 + x^4 + x^3 + x + 1 \)
and find the multiplication \( f(x) \times g(x) \mod m(x) \) using binary arithmetic. Given
\( f(x) = x^7 + x^6 + x^5 + x + 1 \) and \( g(x) = x^7 + x^5 + x^3 + x^2 + 1. \)

1'(b) Using the extended Euclidean algorithm, find the multiplicative inverse of \( 550 \mod 1769 \) and test your result.

2.(a) Explain what are symmetric and asymmetric encryptions. Give any one method of
signature authentication in public key cryptosystem.

2' Explain transposition technique for encryption. If the key used is 4 3 1 2 6 5 7, what
will be the encrypted message of the text “I am going home to come back on two m”
after two transpositions. An encrypted message after single transposition is
E A Y A E D M R X E O O G V O T I S H S G. Decrypt the message using key
6 7 4 5 2 3 1.

3.(a) With the help of block diagram, explain the working of an eight bit PS- LFSR with
[40, 5, 4, 3 ] feedback tappings. What are its advantages over a similar SSRG?

3' With the help of simplified block diagram explain one round of GOST. What are its
advantages and disadvantages over simple DES?

OR

3' With the help of simplified block diagram explain one round of GOST. What are its
advantages and disadvantages over simple DES?

3'(b) Four parallel data streams are to be encrypted and TD Med. Draw the encryption and
decryption schemes using 5 –bit LFSR’s and suitable additional circuits. Briefly explain
the operation of the circuit.

07
4. (a) Show that using a spread spectrum techniques a signal can be transmitted with power below noise power and can be successfully recovered even in the presence of jamming signal. 06

(b) Voice signal at 64 kbps is using DS-SS with PN sequence generated through LFSR with 10-bit shift register. Calculate the clock rate for the LFSR, sequence length, process gain and jamming margin if system loss is 3dB and output signal to noise ratio required is 12 dB. 09

5. (a) [9, 4], [9, 4, 6, 3] and [9, 6, 4, 3], [9, 8, 4, 1] are two preferred feedback pairs for Gold Code generation. Find their cross-correlation bound. Draw the logic block diagram of the circuit using one SSRG and one MSRG so that maximum number of GC sequences are generated. Explain the working of the circuit and discuss its importance for CDMA. 10

(b) Explain FH with diversity. If 8-ary FSK is used with chip repeat factor, N = 5 and bit rate 3 kbps, calculate the minimum separation between the hopping frequencies. 05

OR

(b') What is linear complexity of a random sequence generator? Draw the circuits of Threshold generator and Gollmann Cascade generator and calculate the linear complexities in the two cases if both the circuits are using 3 LFSR's of 5-bit length each. 05
2010-11
II SEMESTER M.TECH. EXAMINATION
ELECTRONICS ENGINEERING
(COMMUNICATION AND INFORMATION SYSTEMS)
ADV. DIGITAL SIGNAL PROCESSING
EL-661

Max. Marks: 75
Notes: Answer any FIVE questions
Make suitable assumptions where necessary.
Symbols used have their standard meanings.

1 a A signal \( x[n] \) is processed by a linear time-invariant system \( H(z) \) and then downsampled by a factor of 2 to yield \( y[n] \) as shown in Figure 1(a). The pole zero plot of \( H(z) \) is shown in Figure 1(b). Determine the pole-zero plot of the system \( G(z) \) shown in Figure 2 such that \( y[n] = r[n] \).

\[ \begin{array}{c}
H(z) \quad \downarrow \quad 2 \downarrow \quad y[n] \\
\text{Figure 1(a)}
\end{array} \]

\[ \begin{array}{c}
2 \downarrow \quad G(z) \quad r[n] \\
\text{Figure 2}
\end{array} \]

1 b Derive the tap weights of LeGall 3/5 synthesis and analysis perfect reconstruction QMF.

2 a Obtain a polyphase decomposition of an IIR system with the transfer function \( H(z) = \frac{1-4z^{-1}}{1+5z^{-1}} \).

2 b Prove that the upsampler by factor-of-L and downsampler by a factor-of-M can be used interchangeably if and only if L and M are relatively prime.

3 a Explain in brief the effect of window length on time and frequency resolution in STFT.

... 2
3 b Derive an expression of weight error vector of an adaptive filter using steepest descent algorithm.

4 a Prove that for an adaptive filter of order M (M is number of taps, very large) using LMS algorithm, the necessary condition on the step size parameter \( \mu \) for convergence in the mean square sense is given by:

\[
0 < \mu < \frac{2}{MS_{\text{max}}}
\]

where \( S_{\text{max}} \) is the maximum value of the power spectral density of the tap inputs.

4 b Calculate the number of complex multiplications and additions required per iteration in an LMS algorithm.

5 Prove that a forward prediction error filter can be changed into a corresponding backward prediction error filter by reversing the sequence in which the tap weights are positioned and taking the complex conjugate of them.

6 A Wiener filter has an input \( u[n] \) and an output \( d[n] \) where

\[
u = [0.7, 0.3]^T \quad d = [0.6]
\]

Variance of the observable data is \( \sigma_u^2 = 0.84 \) and that of additive noise is \( \sigma_d^2 = 0.10 \). Calculate the following:

a. The optimum tap weights of the Wiener filter for order 1 and 2.

b. The minimum mean-square errors for the Wiener filter of order 1 and 2.

7 a Compute the autocorrelation and power spectral density for the signal

\[X(t) = K \cos(2\pi f_c t + \varphi)\]

where \( K \) and \( f_c \) are constants and \( \varphi \) is a random variable which is uniformly distributed over the interval \((-\pi, \pi)\).

7 b Explain how the power spectral density is estimated using the Periodogram method.