2011-2012
M.TECH. (I SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
COMMUNICATION & INFORMATION SYSTEM/
ELECTRONIC CIRCUITS & SYSTEM DESIGN
ADVANCED MATHEMATICS
(AM - 651)

Maximum Marks: 60
Duration: Three Hours

"Students governed by the old ordinances will be examined out of 75 marks and their obtained marks shall be proportionately raised."

Note: Answer any five questions, selecting at least one question from each section.

SECTION – A

1. (a) Define a vector space. Given V(F), a vector space, show that
(i) If a, b ∈ F and α is a non zero vector of V then aα = bα ⇒ a = b.
(ii) If α, β ∈ V and a is a non zero element of F, then aα = aβ ⇒ α = β.

(b) Prove that the vectors (1, 3, 2), (1, -7, -8) and (2, 1, -1) are linearly dependent. (6, 6)

2. (a) If T: V₃(R) → V₃(R) is a linear transformation defined by
T (a, b, c) = (3a, a-b, 2a + b + c), ∀ a, b, c ∈ R. Prove that T is invertible and find T⁻¹.

(b) Define orthogonal vectors. Prove that a set of orthogonal vectors
(1, 0, 0, ....0), (0, 1, 0 .......), (0, 0, 1, 0 ...) ...... (0, 0, 0, ..., 0, 1) in Rⁿ is a linearly independent set.

OR

(b') Let T₁ and T₂ be linear transformations on the finite dimensional vector space, prove that
(i) det (T₁T₂) = det (T₁) det (T₂)
(ii) det (T₁) = 0 ⇔ T₁ is singular

SECTION – B

3. (a) In a bolt factory, machines P, Q and R manufacture 35, 25 and 40 percent of the total output respectively. Of their output 5, 4, 2 percent respectively are defective bolts. A bolt is chosen at random and found to be defective. What is the probability that the bolt came from machine (i) P (ii) Q (iii) R?

Contd......2
(b) The joint probability density function of a two dimensional variable \((X, Y)\) is given by
\[
f(x, y) = \begin{cases} \frac{9(1 + x + y)}{2(1 + x)^4(1 + y)^3}, & 0 < x < \infty \\ 0, & 0 < y < \infty \end{cases}
\]

Find the marginal probability distribution of \(X\) and \(Y\).

4. (a) Show that \(-1 \leq \rho \leq 1\) where \(\rho\) is the correlation coefficient.

(b) Suppose that the two-dimensional continuous random variable \((X, Y)\) has joint pdf given by
\[
f(x, y) = x^2 + \frac{xy}{3}, \quad 0 \leq x \leq 1, \quad 0 \leq y \leq 1
\]

\[
= 0, \text{ else where}
\]

find the marginal pdf of \(X\) and \(Y\)

SECTION – C

5. (a) Show that \(L_n(x) = (-1)^n J_n(x)\)

(b) Prove that
\[
J_n(x) = \frac{1}{\pi} \int_0^\pi \cos(n\phi - x \sin \phi) d\phi.
\]

Where \(n\) is +ve integer.

6. (a) Show that
\[
\frac{1 - z^2}{(1 + 2xz + z^2)^{3/2}} = \sum_{n=0}^{\infty} (2n + 1) P_n'(x)z^n
\]

(b) Prove that
\[
(1 - x^2)P_n' = n(P_{n-1} - xP_n).
\]

7. (a) Show that
\[
\sqrt{1 - x^2} T_n(x) = U_{n+1}(x) - xU_n(x).
\]

(b) Show that \(\frac{1}{\sqrt{1 - x^2}} U_n(x)\) satisfies the differential equation
\[
(1 - x^2) \frac{d^2y}{dx^2} - 3x \frac{dy}{dx} + (n^2 - 1)y = 0
\]

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Answer all questions.
Assume suitable value of data, if it is needed, but not given.

1.(a) Draw the circuit of a comparator and explain its working. Determine the required change in input to switch the output from low to high. Discuss the change of the output from high to low also.

(b) Describe the operation of a comparator as three input NAND, NOR AND and OR gates.

OR

(b') Explain the circuit of a Norton Amplifier and find its voltage gain if the transistors used have $\beta = 80$ and the load resistance is 12 K$\Omega$.

2.(a) Design a Widlar current source for output current $I_0 = 10 \mu A$, when the supply voltage is 10V.

(b) Draw the equivalent circuit and find the output impedance of the above (part-a) current source.

OR

(b') Draw the circuit of cascode mirror, find the expression of its output current when 12V is applied between supply voltage terminal and ground. Calculate the value of the output current when $\beta = 20$ and $I_{\text{ref}} = 1mA$.

3. Figure-1 shows a band-pass filter in which block ‘B’ is a digitally controlled inductor. Explain how you can realize this inductor using (i) OP Amps (ii) OTA’s. Find the transfer function of the filter and give the values of B, W, W_0 and Q of the filter. How can you use this filter as spectrum analyzer?
4. (a) Draw the circuit and explain the working of a voltage controlled quadrature oscillator using OTA's.

(b) A displacement transducer gives output of 100 mV per mm displacement upto 5 mm and 80 mV per mm from 5 mm to 10 mm. Design a signal modifier so that the output is linearly varying between 0 and 1 V as the displacement is varying between 0 to 1 cm.

5. (a) For a simple PLL type I, find the expressions of lock range and capture range.

(b) Draw the block diagram of the PLL and derive the expressions of open loop and closed loop transfer functions. Derive the expression for the B.W. of the PLL.

OR

5' (a) Discuss the frequency synthesizing techniques (i) using PLL (ii) using discreate frequency synthesis.

(b) In a direct frequency synthesizer, one frequency used is 40 MHz and the spectrum generator provides 32 MHz, 38 MHz, 44 MHz and 50 MHz which can be selected digitally. Find the 16 frequencies which can be generated using two-stage frequency synthesizer.
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Instructions to the examinees:
1. Answer any FIVE questions.
2. Make suitable assumptions, if required.
3. Symbols and notations used carry their usual meanings.

<table>
<thead>
<tr>
<th>Question</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q. 1</td>
<td>Design a 3-input XOR gate using Static CMOS Logic. Provide transistor W/L ratios for the designed circuit assuming that $(W/L)_n = 2$, $(W/L)_p = 5$ and the channel length is 32nm.</td>
</tr>
<tr>
<td>Q. 2 (a)</td>
<td>Consider the following statement: <strong>NAND gates are generally preferred for implementing combinational logic functions in CMOS.</strong> Is the above statement TRUE or FALSE? Give examples and reasons to support your answer.</td>
</tr>
<tr>
<td>Q. 2 (b)</td>
<td>Give the transistor level implementations of a 2-input OR/NOR gate and a 2-input AND/NAND gate in Complementary Pass Transistor Logic (CPL). What are the advantages offered by CPL over Static CMOS Logic design?</td>
</tr>
<tr>
<td>Q. 3 (a)</td>
<td>With the aid of a Gajski-Kuhn Y-chart, explain the various description domains and abstraction levels for an integrated circuit.</td>
</tr>
</tbody>
</table>
| Q. 3 (b) | Define the following design techniques in the context of integrated circuit design:  
  i. Hierarchy  
  ii. Regularity  
  iii. Modularity  
  iv. Locality |
| Q. 4     | Explain the difference between:  
  i. Sea-of-Gates and Gate Arrays  
  ii. Programmable Logic Array (PLA) and Programmable Array Logic (PAL)  
  iii. Standard Cell Design and Full Custom Design |
| Q. 5 (a) | Giving the internal details of the routing cell and explain how signals are routed in an **ACTEL** FPGA. Also discuss the significance of ‘Personalization RAM’. |
| Q. 5 (b) | Draw the internal diagram of an **ACTEL** FPGA logic cell and explain its working by configuring the built-in 16*1 RAM for obtaining the logic function $(A \ XOR \ B \ XOR \ C \cdot D)$ where $A$, $B$, $C$ and $D$ are the inputs to the logic cell. |
| Q. 6 (a) | Using suitable block diagrams, explain the operation of the Configurable Logic Block (CLB) used in **XILINX Spartan** series FPGA. |
| Q. 6 (b) | How can the Look-Up Tables provided in the CLB of **XILINX Spartan** series FPGA be used to implement a 5-input combinational logic function. |
| Q. 7 (a) | With the help of suitable examples, explain the difference between logic verification, silicon debug and manufacturing test. |
| Q. 7 (b) | Discuss the Scan-based approach to Design for Testability in digital integrated circuits. |
I SEMESTER M.TECH. EXAMINATION 2011-12
ELECTRONICS ENGINEERING
IC PROCESSES AND FABRICATION
EL-623

Max. Marks: 60
Time: Three Hours

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Attempt ANY FIVE Questions

1 a What is the need of ultra clean environment for the fabrication of Integrated Circuits? Describe the class- 1 cleanliness. What are the Do’s and Don’ts for the clean room. What are the sources of contaminations?

1 b Briefly describe the specifications, installations, operations and automation of HEPA Filters. What are the common design practices for clean rooms?

2 a What is the importance of ultra clean water for an IC lab? What are the constituents of ground water? How ultra clean water is obtained for IC Lab?

2 b Differentiate between wet cleaning and dry cleaning? Explain in detail wet cleaning process.

2 c Why Si is preferred over Ge? How the pure Silicon is obtained from Silica?

3 a Briefly describe the advantages and disadvantages of Physical Vapour Deposition (PVD). How PVD is different from Chemical Vapour Deposition (CVD)? With sketches, explain the operation of Vacuum Evaporation System. How alloys are deposited using Vacuum Evaporation System.

3 b Assume that the gas SiH$_4$ is introduced into a reactor and that the only chemical reaction that occurs in the chamber is

\[ \text{SiH}_4 (g) \rightleftharpoons \text{SiH}_2 (g) + \text{H}_2 (g) \]

If the process is run at 1 atm (760 torr) and temperature of 1000 K the process reaches chemical equilibrium, calculate the partial pressure of each species. The equilibrium constant for the reaction is given by

\[ K_p(T) = 1.6 \times 10^9 \ e^{-2/kT} \]

4 a With sketches, explain the operation of Sputtering System.
4b What are the applications of silicon dioxide. With the help of sketch, explain the growth of silicon dioxide. A 100 A gate oxide is required for some technology. It has been decided that the oxidation will be carried out at 1000 °C, in wet ambient. If there is no initial oxide, for how long should the oxidatiob be done? Is the oxidation in the linear regime, the parabolic regime or between the two? (A=0.226, B=0.287, τ = 0.37 hr).

5a Why low temperature processes are preferred in IC fabrication? With the help of sketch, explain the operation of a typical LPCVD system.

5b Describe the photolithography process step by step with the help of sketches. What is the difference between isotropic and anisotropic etching?

5c What are the advantages of ion implantation over classical diffusion method. With the help of sketch, explain the operation of a typical ion implantation system.

6 With the help of sketches, explain the all fabrication steps of CMOS Inverter.

7 With the help of sketches, explain the all fabrication steps of monolithic Bipolar integration process by taking a simple circuit.
2011-2012
M.TECH. (I SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
DIGITAL SYSTEM DESIGN USING HDL
(EL-626)

Maximum Marks. 60
Duration: Three Hours

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Answer all questions. Make suitable assumptions wherever necessary.

1(a) Write a synthesizable Verilog code and a testbench for a 4-bit by 4-bit signed multiplier by using the multiplier operator.

OR

1'(a) Write a Verilog code and a test bench of a dual port RAM having sixteen locations each of 8-bits.

1(b) Explain briefly assertion based verification and formal verification? What is their advantages over purely simulation based verification?

2(a) What is meant by triangular optimization in VLSI Design? Explain the three important parameters which are usually optimized.

2(b) Explain the different steps involved in the design of a Field Programmable Gate Array based Digital System.

3(a) Realise a following function of three variables with the help of logic cells shown in Figure 1.

\[ F(x,y,z) = \Sigma(0,1,3,5,7) \]

OR

3'(a) Realise a following function of three variables with the help of logic cells shown in Figure 2.

\[ F(x,y,z) = \Sigma(1,2,4,6) \]

3(b) Compare different implementation technologies in terms of cost, speed, flexibility and power consumption.

3(c) What is the difference between a Xilinx FPGA and a CPLD?

4(a) Explain the architecture that implements the following function by using three multipliers and three adders.

\[ P_s(x) = \sum_{i=0}^{s} px_i \]

4(b) Write a Verilog code for the data subsystem shown in Figure 3.
5(a) Write a microprogram to count the number of 0's in the lower nibble of a 1-byte input vector for the data system shown in Figure 3. Assume that the ALU supports only ADD, SUB and XOR operations. Write the Verilog code of the control unit as well.

OR

5'(a) Write a microprogram to count the number of 0's in the upper nibble of a 1-byte input vector for the data system shown in Figure 3. Assume that the ALU supports only ADD, SUB and INC operations. Write the Verilog code of the control unit as well.

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Figure 1

Figure 2

Figure 3
I Semester M Tech Examination
(Engineering)
INFORMATION AND CODING THEORY
(EL – 651)

Maximum Marks: 60
Duration: Three Hours

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Answer any FOUR questions.

1. (a) List all primitive elements of $GF(8)$.
   (b) Determine the generator polynomial and the code rate of a double-error correcting Reed-Solomon code with block length $n = 7$. How many codewords does this code have?
   (c) A two-state Markov chain has a transition matrix
   \[ P = \begin{bmatrix} 1 - \alpha & \alpha \\ \beta & 1 - \beta \end{bmatrix} \]
   (i) Find the entropy rate.
   (ii) What values of $\alpha, \beta$ maximize the rate of part (i)?

2. (a) Differentiate between a regular and an irregular LDPC code. Give an algorithm for algebraic construction of LDPC codes.
   (b) Show that when a binary sequence $c$ of length $n$ is transmitted over a binary symmetric channel (BSC) with cross over probability, $p$, the probability of receiving $v$, which is at Hamming distance $d$ from $c$, is given by
   \[ P(v | c) = (1 - p)^n \left( \frac{p}{1 - p} \right)^d. \]
   If $p < 1/2$, show that $P(v | c)$ is a decreasing function of $d$ and hence ML decoding is equivalent to minimum Hamming distance decoding. What happens if $p > 1/2$?

3. (a) Let $\alpha$ be a primitive element of $GF(2^4)$. Show that $\{0,1, \alpha^5, \alpha^{10}\}$ is a field.
   (b) A $(k+1, k)$ block code is generated by adding one extra bit to each information sequence of length $k$ such that the overall parity of the code (i.e., the number of 1s in each codeword) is an odd number. Two students, A and B, make the following arguments or error detection capability of the code
   1. Student A: Since the weight of each codeword is odd, any single error changes the weight to an even number. Hence, this code is capable of detecting any single error.
   2. Student B: The all-zero information sequence $00 \ldots 0$ will be encoded by adding one extra 1 to generate codeword $00 \ldots 01_k$. This means that there is at least one codeword of weight 1 in this code. Therefore $d_{\text{min}} = 1$, and since code can detect at most $d_{\text{min}} - 1$ errors, this can code can not detect any errors.
   Which argument do you agree with and why? Give your explanation in one short paragraph.
(c) Consider a series of $M$ BSCs, each with crossover probability $p$, where the output of each BSC is connected to the input of the next in the series. Show that the resulting overall channel is a BSC and determine the crossover probability as a function of $M$.

4. (a) Let $f(x) = x^{10} + x^9 + x^5 + x^4$ and $g(x) = x^2 + x + 1$ be the polynomials in $GF(2)[x]$. Write $f(x) = g(x)q(x) + r(x)$, where $\deg r(x) < \deg g(x)$.

(b) Draw a trellis representing the binary block code described by the following check matrix

$$ H = \begin{bmatrix} 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix} $$

(c) The sample function of a Gaussian process of zero mean and unit variance is uniformly sampled and then applied to a uniform quantizer having the input-output amplitude characteristics as shown in Fig 1. Calculate the entropy of the quantizer output. Use $\text{erf}(4/\sqrt{2}) = 0.6778$.

5. (a) Define a convex function. Show that the binary entropy function $H_2(p)$ is concave on $(0, 1)$.

(b) Show that in $GF(2)$, $g(x) = (x^{11} + 1)(x^6 + x + 1)$ is a valid generator polynomial of a Fire code. What is the burst error correction length for this code?

(c) A trellis coded signal is formed as shown in Fig 2 by encoding each bit by the use of a rate-1/2 convolutional code while 3 additional information bits are left uncoded. Perform the set partitioning of 32-QAM (cross) constellation, and indicate the subsets in the partition. By how much is the distance between adjacent signal points increased as a result of partitioning.

Fig 1

Fig 2
6. (a) How many primitive elements are in $GF(32)$?
(b) Let $X^n$ be iid $\sim p(x)$. Let $\varepsilon > 0$. Prove that there exists a code which maps sequences $X^n$ of length $n$ (sufficiently large) into binary strings such that the mapping is one to one and $E\left[\frac{1}{n}l(X^n)\right] \leq H(X) + \varepsilon$.
(c) The trellis diagram of a binary convolutional encoder is shown in Fig - 3. A sequence output by the encoder is transmitted over a channel subject to random errors, and is received as the sequence 11 10 11 00 11 ....
   (i) Using the Viterbi algorithm, find the sequence most likely to have been transmitted.
   (ii) A sequence from the encoder of (i) is transmitted over additive white Gaussian noise channel and is received as 33 10 23 00 33 ... after soft detection with four levels. Find the most likely error pattern in received sequence.

![Trellis Diagram](image)
1. (a). Let a scattering function \( S_c(\tau, \rho) \) be nonzero over \( 0 \leq \tau \leq 0.1 \) ms and \(-0.1 \leq \rho \leq 0.1 \) Hz. Assume that the power of the scattering function is approximately uniform over the range where it is nonzero.

i. What are the multipath spread and the Doppler spread of the channel?

ii. Suppose you input to this channel two identical sinusoids separated in time by \( \Delta t \). What is the minimum value of \( \Delta f \) for which the channel response to the first sinusoid is approximately independent of the channel response to the second sinusoid.

iii. For two sinusoidal inputs to the channel \( u_1(t) = \sin(2\pi f t) \) and \( u_2(t) = \sin(2\pi f(t+\Delta t)) \), what is the minimum value of \( \Delta t \) for which the channel response to \( u_1(t) \) is approximately independent of the channel response to \( u_2(t) \).

iv. Will this channel exhibit flat fading or frequency-selective fading for a typical voice channel with a 3 KHz bandwidth? How about for a cellular channel with a 30 KHz bandwidth?

(b). Drive an expression for Shannon capacity of a fading channel when channel state information is known to both the transmitter and receiver.

OR

(b'). Consider a flat-fading channel of bandwidth 20 MHz where for a fixed transmit power, the received SNR is one of six values: \( \gamma_1 = 20 \) dB, \( \gamma_2 = 15 \) dB, \( \gamma_3 = 10 \) dB, \( \gamma_4 = 5 \) dB, \( \gamma_5 = 0 \) dB and \( \gamma_6 = -5 \) dB. The probability associated with each state is \( p_1 = p_6 = .1, p_2 = p_4 = .15, \) and \( p_3 = p_5 = .25 \). Assume only the receiver has CSI. Find the capacity versus outage for \( 0 \leq P_{out} < 1 \).
2. (a). Determine the probability density function of received SNR per symbol for Rayleigh fading channel.

OR

(a'). Derive the expression for moment generating function for Rayleigh fading.

(b). Find a closed-form expression for the average probability of error for DPSK modulation in Nakagami-m fading. Evaluate for $m = 4$ and $\tilde{\gamma}_b = 10$ dB.

(c). Drive an expression for SNR at the combiner output for maximal ratio combining (MRC) diversity.

OR

(c'). Show that when channel gains are known to the transmitter, transmit diversity is very similar to receiver diversity with MRC.

3. (a). Consider a wireless communication system with two-antenna transmit diversity employing Alamouti's scheme. Show how to recover the transmitted symbols and achieve dual diversity reception.

(b). Determine the capacity of a MIMO system when CSI is unknown at the transmitter.

OR

(b'). Consider a 2×2 MIMO system with channel gain matrix $\mathbf{H}$ given by

$$ \mathbf{H} = \begin{bmatrix} .3 & .5 \\ .7 & .2 \end{bmatrix} $$

Assume $\mathbf{H}$ is known at both the transmitter and receiver, and that there is a total transmit power of $P = 10$ mW across the two transmit antennas, AWGN with power $N_0 = 10^{-3}$ W/Hz at each receive antenna, and bandwidth $B = 100$ KHz. Find the capacity of this channel.

4. (a). It is required to design a system with user data rate of 1Mbps. Typical outdoor channels show RMS delay spread $\sigma$, of 10μs. Determine whether ISI will occur in a single carrier system? If yes, propose a multicarrier system that would avoid ISI. Please note that channel coherence bandwidth is defined as, $B_c = 1/5\sigma$ and frequency selectivity occurs when $\sigma < \text{symbol duration}/10$.

(b). What are the key features of OFDM which make it suitable for broadband wireless communications?

(c). What are the advantages of CDMA access techniques for mobile system?
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Answer any FIVE Questions. Assume suitable data if missing

Q1(a) What are radar beacons? What applications do they have? (5 marks)

Q1(b) The radar antenna diameter is 1000ft, it has a transmitted pulse power of 40Mw, the frequency is 2.4 Ghz, the bandwidth is 10 Hz. The transponder has an 8-ft diameter paraboloid reflector antenna, and a receiver noise figure of 4.77 dB, what is the maximum range for interrogation link? (7 marks)

Q2(a) Discuss the propagation of radar waves on flat earth. (5 marks)

Q2(b) Consider a low PRF radar at a height of 2000ft and a target at a height of 20,000ft with a radar target range of 30nmi. Calculate the length of the reflected path and the angle of incident. (7 marks)

Q3 What is a synthetic aperture radar? What are its applications? (12 marks)

Q4 Explain the working of Track while scan radar with necessary illustrations. (12 marks)

Q5 What are hyperbolic systems? Discuss any two of them. (12 marks)

Q6 With the help of necessary illustrations describe the working of instrument landing system. (12 marks)

Q7 Discuss the relative merits and demerits of Doppler and satellite navigation system. (12 marks)
1 (a) Distinguish between logical address and port address.

(b) A long distance point-to-point data link uses an idle (stop-and-wait) ARQ strategy with half-duplex transmission and has the following characteristics: Data transmission rate = 5.4 kbps, Frame size = 896 bits, Propagation delay = 10 ms. If processing delays and acknowledgement transmission time can be neglected, determine the link utilization: (i) in the absence of errors and (ii) in the presence of bit error rate of $10^{-3}$.

(c) A series of 1000-bit frames is to be transmitted using a continuous RQ protocol. Determine the link efficiency for the following types of data link if the velocity of propagation is $2 \times 10^8$ m/s and the bit error rates of the link are all negligibly low:
(i) A 1 Km link of 1 Mbps and a send window $K=2$
(ii) A 10 Km link of 200 Mbps and a send window $K=7$

2 Two CSMA/CD stations are each trying to transmit long (multi-frame) files. After each frame is sent, they contend for the channel, using binary exponential back-off algorithm. What is the probability that the contention ends on round $k$, and what is the mean number of rounds per contention period?

3 (a) Give the values of operational parameters of standard Ethernet.

(b) Explain the significance of keeping a certain minimum frame size for Ethernet.

(c) Distinguish between the signaling schemes used in 100Base-T4 and 100Base-TX.

4 (a) Explain the difference between the following two types of Ethernet switches: Store-and-forward switch and Cut-through switch.

(b) What are the different physical layer techniques used in various IEEE802.11 standards?

(c) Distinguish between hidden station problem and exposed station problem encountered in Wireless networks.
5 (a) Describe briefly the three power classes in the Bluetooth standard?

(b) Most Bluetooth devices operate at a transmission rate of 1 Mbps, but the actual throughput obtained is much lower. Give reasons for this.

(c) With regard to Bluetooth, (i) distinguish between SCO and ACL type of links, (ii) distinguish between piconet and scatternet.

6 (a) What is Dijkstra's Shortest Path algorithm?

(b) Give a brief account of Open loop congestion control techniques used at the network layer.

(c) Explain briefly why a lot of address space is wasted using classless addressing in IPv4.