2010-2011
M.TECH. (I SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
COMMUNICATION & INFORMATION SYSTEM/
ELECTRONIC CIRCUITS & SYSTEM DESIGN
ADVANCED MATHEMATICS
(AM – 651)

Maximum Marks: 75

Duration: Three Hours

Note: Answer any five questions, selecting at least one question from each section.

SECTION – A

1 (a) Define a Vector space. Show that a non-empty subset \( W \) of a vector space \( V \) over a field \( F \) is a subspace of \( V \) if and only if, for all \( \alpha, \beta \in F \) and \( x, y \in W \), \( \alpha x + \beta y \in W \).

(b) Prove that the vectors \((1,0,1), (1,1,0) \) and \( (1,1,1) \) are linearly independent. \( (8+7) \)

2 (a) If \( T : V_3(\mathbb{R}) \rightarrow V_2(\mathbb{R}) \) is a linear transformation defined by

\[
T (a, b, c) = (a+b, 2c-a) \text{ and}
\]

\[
B_1 = \{ (1,0,-1), (1,1,1), (1,0,0) \}
\]

\[
B_2 = \{ (0,1), (1,0) \}
\]

are bases of \( V_3(\mathbb{R}) \) and \( V_2(\mathbb{R}) \) respectively, find the matrix of \( T \) relative to the bases \( B_1 \) and \( B_2 \).

(b) Define orthogonal vectors. Prove that a set of orthogonal vectors in \( \mathbb{R}^n \) is a linearly independent set. \( (8+7) \)

SECTION – B

3 (a) Suppose that the two – dimensional continuous random variable \((X,Y)\) has joint pdf given by

\[
f(x,y) = x^2 + \frac{1}{3} xy, \quad 0 \leq x \leq 1, 0 \leq y \leq 2
\]

\[
= 0, \text{ else-where}
\]

find the marginal pdf of \( X \) and \( Y \).

(b) In a bolt factory, machines \( P, Q \) and \( R \) manufacture 35, 25, 40 percent of the total output respectively. Of their output 5, 4, 2 percent respectively, are defective bolts. A bolt is chosen at random and found to be defective. What is the probability that the bolt came from machine (i) \( P \) (ii) \( Q \) (iii) \( R \)?
4 (a) Suppose that two dimensional random variable \((X, Y)\) has Joint pdf.
\[ f(x, y) = Kx(x-y), \quad 0 < x < 2, \quad -x < y < x \]
\[ = 0. \]
(i) Evaluate the constant \(K\)
(ii) Evaluate the marginal pdf of \(X\)
(iii) Evaluate the marginal pdf of \(Y\).
(b) If \(\psi_1^2\) and \(\psi_2^2\) are two independent chi-square distributions with parameters \((8+7)\)
having \(n_1\) and \(n_2\) degree of freedom, then show that \(\psi_1^2 + \psi_2^2\) is a chi-square
distribution with \((n_1+n_2)\) degree of freedom.

SECTION - C

5 (a) Prove Rodrigue’s formula
\[ P_n(x) = \frac{1}{2^n \ln} \frac{d^n}{dx^n} (x^2 - 1)^n \]
(b) Prove that
\[ (2n+1)(x^2 - 1) P_n^1 = n(n+1) (P_{n+1} - P_{n-1}) \] \hspace{1cm} \text{(7+8)}

6 (a) Show that \(J_{-n}(x) = (-1)^n J_n(x)\)
(b) Express \(\int J_3(x) dx\) in terms \(J_0\) and \(J_1\)

7 (a) Show that
\[ \sum_{n=0}^{\infty} T_n(x) = \frac{1}{2} \left[ \frac{1}{U_{2n+1}(x)} \right] \]
(b) Prove that
\[ (T_n(x))^2 - T_{n+2}(x) T_{n-1}(x) = 1 - x^2 \] \hspace{1cm} \text{(7+8)}

*****
1. (a) Draw the circuit of a Wilson current source and find the expression of its output current in terms of $I_{ref}$ and $\beta$. If the transistors used are matched but $V_{BE}$ is changed from 0.65 V to 0.7 V, what will be the corresponding change in the output current? Take $V_{CC} = +5V$, $V_{EE} = -5V$, $RC = 10k\Omega$ and $\beta = 150$. The terms carry their usual meaning.

(b) Draw the circuit of a differential amplifier using a Wilson current mirror as its active load. Show that its output impedance is $R_o = \frac{\beta r_o}{\beta + 2}$ where $r_o$ is the output impedance of a transistor.

OR

(b') For the CMOS differential amplifier with active load as shown in Figure 1, show that the voltage gain,

$$A_v = \frac{V_A}{V_{os} - V_i}$$

where $V_A$ is positive voltage similar to Early voltage in BJT's. The other terms carry their and meaning.

![Fig. 1.](image)

2. (a) Explain the working of CFA as an inverting and a non inverting amplifier. Find the expression of the B.W. considering a capacitive load.

(b) If the maximum band width is 100 MHz when the mid band gain is $= -30$. What will be the B.W. if the input resistance $r_i = 10\Omega$ and feedback resistance is $1.5k\Omega$? Derive the formula used. What will be the B.W. if the mid band gain is doubled.

Contd…..2
(b') Draw the circuit and explain the working of (i) voltage controlled current sink, (ii) voltage controlled current source using a Norton Amplifier. Give the advantages and disadvantages of Norton amplifier. As compared to simple OP Amp.

3

Do any two of the following:

(a) Draw the circuit and explain the working of an electronically controlled impedance multiplier using OTA. (06)

(b) Draw the circuit and explain the working of digitally controlled inductance realization using OP Amps. (06)

(c) With the help of the circuit realized in part (a) or part (b) explain how you can realize an electronically controlled band pass filter. (06)

4

(a) A PLL is using polar X-OR as its phase detector. The maximum voltage of the phase detector is $v_{\text{max}} = \pm 0.7V$ and the low pass filter gain, $A = 2$. Find the lock range if the free running frequency, $f_0 = 50kHz$. Take VCO sensitivity, $k_v = 25kHz/V$. Derive the formula used. (05)

(b) Draw the block diagram of the linear model of type I PLL. Find its close loop transfer function and the expression of open loop unity gain frequency and close loop band width. (10)

OR

(b') Draw the circuit of a multiple loop frequency synthesizer. Explain its working taking an example of realizing frequency in the range of 15MHz to 20.5MHz in steps of 2kHz. Take reference frequency $f_r = 100$ kHz. (10)

5

(a) Discuss the operation of class C amplifier and show that its efficiency is more than 78.5% and it can be controlled by controlling the conduction angle. (08)

(b) Discuss the class C amplifier as frequency multiplier. Find the conduction angle if the amplifier is to be used as a frequency tripper. (07)

OR

(b') Discuss the operation of Class D amplifier and find the expressions of its efficiency and the harmonic components present in its output. (07)

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Maximum Marks: 75

Note:  (i) Attempt only four questions.
      (ii) Q.No. 1 is compulsory.

1. (a) What is the desirable input and output impedance for active current mode and 
      voltage mode filters? Justify your answer.  (04)

1. (b) Realize an ideal differentiator using OTAs and grounded capacitor. Also give 
      the attractive feature of the circuit.  (05)

1. (c) Show that the network of figure 1 realizes an ideal grounded inductor. Design 
      the same for 10mH, assuming C = 10nF.  (06)

2. (a) Give the realization of grounded parallel RL-simulator using OTA. Also use it 
      to realize second order high pass gm-C filter. Analyse the incremental 
      sensitivities for the pole \( -\omega_0 \), Pale-Q and gain of the filter.  (12)

2. (b) Design the gm-C biquadratic filter of part (a) for pale frequency of 300 kHz 
      and Pale-Q = 5   (08)

3. Give gm-C realization of 8th order prototype band pass ladder filter using Leap 
   Frog technique.  (20)

4. (a) How can we realize (i) Voltage follower (ii) Current follower using CCII?  (06)

4. (b) What do you understand by Cascade Realization?  (04)

4. (c) Realize load insensitive current mode first order low pass, high pass and all 
      pass filter sections using CCII. Give their pale frequencies and gains. Also 
      analyze the incremental sensitivities of various filter parameters.  (10)

5. (a) Realize grounded and floating resistor using only CCCII.  (04)

5. (b) Realize an ideal grounded inductor using CCCII and capacitor only. Use the 
      realized inductor in the realization of low pass, high pass and band pass filter. 
      Also give the expression for pale frequency, pale-Q and gain of the filters. 
      Write attractive features of the circuit.  (10)

5. (c) Design the band pass filter of part (a) for pale frequency of 50kHz and pale-Q 
      of 20.  (06)

6. (a) What are the advantages and limitations of switched capacitor filters.  (06)

6. (b) Give the switched capacitor realization of resistor and integrating summer.  (06)

6. (c) Show the implementation of a double-poly integrated capacitor and its small 
      signal model. How does the parasitic capacitances affect switched capacitor 
      integrator?  (08)

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Figure enclosed.
Q. 1 (a) Consider an inverter implemented in Pseudo-NMOS logic. What will be the effect of altering the size of the PMOS transistor (while keeping the size of NMOS transistor fixed) on the voltage-transfer characteristics? 6

Q. 1 (b) Draw the circuit for a BICMOS inverter with
   (i) Passive bleeding elements 9
   (ii) Active bleeding elements

   What are the advantages offered by the BICMOS inverter over a CMOS inverter implemented in static CMOS technology.

Q. 2 (a) Describe all types of power dissipation in integrated circuits. 6
Q. 2 (b) Give the transistor level implementations of a 2-input XOR/XNOR gate in Differential Cascode Voltage Switch Logic (DCVSL) and Complementary Pass Transistor Logic (CPL). What are the advantages offered by the latter over the former? 9

Q. 3 (a) With the aid of a Gaajski-Kufln Y-chart, explain the various description domains and abstraction levels for an integrated circuit. 7
Q. 3 (b) Define the following design techniques in the context of integrated circuit design:
   i. Hierarchy
   ii. Regularity
   iii. Modularity
   iv. Locality

Q. 4 Write short technical notes on the following VLSI Design Methodologies: 15
   i. Sea of Gates & Gate Array
   ii. Programmable Logic Array (PLA)
   iii. Complex Programmable Logic Devices (CPLD)
   iv. Standard Cell Design
   v. Full Custom (ASIC) Design

Q. 5 (a) Give the floorplan of a typical ACTEL FPGA chip. Further, show the internal details of the routing cell. 6
Q. 5 (b) Draw the internal diagram of an ACTEL FPGA logic cell and explain its working by configuring the built-in 16x1 RAM for obtaining the logic function \( \sum(A,B,C,D) \) where A, B, C and D are the inputs to the logic cell. 9

Q. 6 Using suitable block diagrams, explain the operation of the Configurable Logic Block (CLB) and the input-output block (IOB) used in XILINX Spartan series FPGA. 15

Q. 7 (a) With the help of suitable examples, explain the difference between logic verification, silicon debug and manufacturing test. 6
Q. 7 (b) Discuss the Scan-based approach to Design for Testability in digital integrated circuits. 9
2010-2011
M.TECH. (I SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
DIGITAL SYSTEM DESIGN USING HDL
(EL-626)

Maximum Marks:75

Duration: Three Hours

Answer all questions.

1(a) Write a synthesizable Verilog code for a 4-bit by 4-bit unsigned multiplier by executing shift and add operations in a sequence in the datapath. The control unit of the multiplier should be realized by using a Finite State Machine. (10)

OR

1'(a) Write a Verilog code and a test bench of a LIFO having sixteen locations each of 8-bits. (10)

1(b) Explain briefly the concept of assertion based verification? What is its advantage? (3+2)

2(a) What is meant by triangular optimization in VLSI Design? Explain the three important parameters which are usually optimized. (2+3)

2(b) Explain the different steps involved in the design of application specific integrated circuit. (10)

3(a) Realise a following function of four variables with the help of logic cells shown in Figure 1.

\[ F(w,x,y,z) = \Sigma(1,3,7,9,10,12,14,15) \]

OR

3'(a) Realise a following function of four variables with the help of logic cells shown in Figure 2.

\[ F(w,x,y,z) = \Sigma(1,2,7,9,10,11,14,15) \]

3(b) Compare different implementation technologies in terms of speed, flexibility and power consumption. (5)

3(c) What is the difference between SRAM based FPGA and CPLDs (3)

4(a) Explain the RTL of the architecture that implements the following function

\[ P_s(x) = \sum_{i=0}^{3} px^i \]

by using a processor that consists of a multiplier and an adder. (8)

4(b) Write a Verilog code for the data subsystem shown in Figure 3. (7)
5': Write a microprogram to count the number of 1's in a lower nibble of a 1-byte input vector for the data system shown in Figure 3. Assume that the ALU supports only ADD, SUB and XOR operations. Write the Verilog code of the control unit as well. (15)

OR

5': Write a microprogram to count the number of 1's in the upper nibble of a 1-byte input vector for the data system shown in Figure 3. Assume that the ALU supports only ADD, SUB and INC operations. Write the Verilog code of the control unit as well. (15)
2010 – 2011
I Semester M Tech Examination
(Electronics Engineering)
INFORMATION AND CODING THEORY
(EL – 651)

Maximum Marks: 75
Duration: Three Hours

Notes:
1. Answer any FIVE questions.
2. Any missing information can suitably be assumed.

1. (a) Does the set of all integers (positive, negative and zero) form a group under subtraction? Explain.
(b) A certain source has eight symbols, and emits data in blocks of three symbols at the rate 1000 blocks/s. The first symbol in each block is always the same for synchronization purposes; the remaining two places are filled by any of eight symbols with equal probability. Find the source information rate.
(c) For the RM(1, 4) code:
   (i) Write the generator matrix G.
   (ii) Determine the minimum distance of the code.

2. (a) Construct the addition and multiplication tables for \( F[x]/\langle x^2 + 1 \rangle \) defined over \( GF(3) \).
(b) Find the codeword for the single-error-correcting Reed-Solomon code of block length 15 based on primitive element \( \alpha \) of \( GF(2^4) \) that corresponds to the data polynomial \( \alpha^5 x + \alpha^3 \).
(c) Consider a source \( X \) uniformly distributed on the set \( \{1, 2, \ldots, m\} \). Find the rate distortion function for this source with Hamming distortion defined as

\[
d(x, \bar{x}) = \begin{cases} 
0 & x = \bar{x} \\
1 & x \neq \bar{x}
\end{cases}
\]

3. (a) A modified cumulative distribution function of a discrete random variable, \( X \), is defined as

\[
\bar{F}(x) = \sum_{\alpha < x} p(\alpha) + \frac{1}{2} p(x),
\]
where \( p(x) \) is the probability mass function. Can you use the value of \( \bar{F}(x) \) as a code for \( x \). What happens if \( \bar{F}(x) \) needs infinite number of bits for its representation?
(b) Draw a Tanner graph of an LDPC code described by the following check matrix and decode the received vector \( v = (1 1 0 1 0 1 0 1) \)

\[
H = \begin{bmatrix}
0 & 1 & 0 & 1 & 0 & 0 & 1 \\
1 & 1 & 1 & 0 & 0 & 1 & 0 \\
0 & 0 & 1 & 0 & 0 & 1 & 1 \\
1 & 0 & 0 & 1 & 1 & 0 & 1
\end{bmatrix}
\]
4. (a) Find a generator matrix $G(x)$ for the convolutional encoder shown in Figure 1.

(b) A memoryless ternary source with output alphabet $a_1, a_2$ and $a_3$ and corresponding probabilities 0.2, 0.3, 0.5 produces sequences of length 1000.
(i) What is the approximate number of typical sequences in the source output?
(ii) What is the ratio of typical sequences to atypical sequences?
(iii) What is the number of bits required to represent all output sequences?
(iv) Which one is the most probable sequence and what is its probability?

5. (a) Does a vector space exist with 24 elements over some finite field $GF(q)$?
(b) Draw the trellis diagram for a linear block code described by the following check matrix

\[ H = \begin{bmatrix}
1 & 0 & 1 & 0 & 0 \\
0 & 1 & 0 & 1 & 0 \\
0 & 1 & 1 & 0 & 0
\end{bmatrix} \]

(c) A continuous random variable $X$ is constrained to a peak magnitude $M$, that is $-M < X < M$.
(i) Show that the differential entropy of $X$ is maximum when the pdf of $X$ is given as: $f_X(x) = \begin{cases} 
\frac{1}{2M} & -M < x \leq M \\
0 & \text{otherwise}
\end{cases}$
(ii) Show that the maximum differential entropy of $X$ is $\log_2 2M$.

6. (a) Let $X_i$ be uniformly distributed over the states \{0, 1, 2\}. Let $\{X_i\}_i^\infty$ be a Markov chain with transition matrix $P$ defined as
$P = [P_{ij}] = P[X_{n+1} = j | X_n = i]$, $i, j \in \{0,1,2\}$
and given by

\[ P = \begin{bmatrix}
1/2 & 1/4 & 1/4 \\
1/4 & 1/2 & 1/4 \\
1/4 & 1/4 & 1/2
\end{bmatrix} \]
(i) Is $\{X_n\}$ stationary?
(ii) Find the entropy rate.
(b) Consider a rate $2/3$ convolutional code defined by the following generator polynomial matrix

$$G(x) = \begin{bmatrix} 1 & x & x + x^2 \\ x^2 & 1 + x & 1 + x + x^2 \end{bmatrix}$$

This code is used with an 8-PSK signal set that uses Gray coding. The bandwidth efficiency of this TCM scheme is 2 bits/s/Hz.

(i) How many states are there in the trellis diagram for this encoder?
(ii) Find the free Euclidean distance.
(iii) Find the asymptotic coding gain with respect to uncoded QPSK, which has a bandwidth efficiency of 2 bits/s/Hz.

7. (a) Show that the linear block code defined over $GF(2)$ with check matrix

$$\begin{bmatrix} 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}$$

is self-dual.

(b) Design $(6, 2)$ cyclic code over $GF(2)$ by choosing the shortest possible generator polynomial.

(i) Generate code $C$ in the systematic form.
(ii) How many errors can be corrected by the code?
(iii) If code is used in conjunction with BPSK over an AWGN channel with average signal power $P = 1W$, noise power spectral density, $N_0 = 2 \times 10^{-6}$ W/Hz and channel bandwidth, $W = 6 \times 10^4$ Hz and the information is transmitted at the maximum theoretically possible speed, find the upper bound on probability of error assuming receiver is employing soft decision decoding. Take $Q(\sqrt{4.1667}) = 2.063 \times 10^{-2}$.

Given that over $GF(2)$, $x^6 + 1 = (x + 1)^3(x + 1)^3$.

8. (a) For the $(n, 1)$ code used over BSC with crossover probability $p$, what is the probability that an error event occurs which is not detected?

(b) For a BSC with crossover probability $p$ having input $X$ and output $Y$, let the probability of the input be $P[X=0]$. Show that the channel capacity per channel use is $C = 1 - H_2(p)$ bits.

(c) A $(3, 1)$ code consists of two codewords $000$ and $111$. The codewords are transmitted using BPSK with bit energy $E_b = 1$. The received vector (sampled output of the matched filter) is $r = (0.5, 0.5, -3)$. Find the transmitted codeword with (i) soft decision decoder (ii) hard decision decoder. Are the two results same? If no, which decision should be preferred and why?
2010-2011
M. TECH (I SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)

VOICE AND PICTURE CODING (EL-653)

Maximum Marks: 75

Note: (i) Answer any five questions.
    (ii) Assume any suitable data where necessary.
    (iii) Symbols used carry their usual meanings.

1. (a) With the help of suitable diagrams, explain the working of human visual system.
    (b) Almost all practical speech, audio, image and video coding algorithms use one or other type of quantisers. Why?
    (c) What are the various functions performed by outer, middle and inner parts of human ear in listening sound. Explain how the frequencies of audio signals are discriminated in human ears. At which frequency the ear has maximum sensitivity?

2. (a) A speech signal \( x(t) \) has a probability density function
        \[
        p_x(x) = 1 - |x|, \quad \text{for} \quad -1 \leq x \leq +1
        \]
    This signal is quantized by a quantizer that has eight quantization levels.
    (i) Determine the voltages at which the quantization levels should be located so that there shall be equal probabilities that \( x(t) \) is between any two adjacent levels or between the extreme levels and \( +1 \) and \( -1 \) extreme voltages.
    (ii) If a quantizer is used with equal spacing between quantization levels, make an input-output plot of the compander that must precede the quantizer to satisfy the requirements of part (i).

3. (a) When you enter a dark theater on a bright day, it takes an appropriate interval of time before you can see well enough to find an empty seat. Which of the visual process is at play in this situation?

(b) How is temporal masking useful in speech coding? Differentiate between pre-
masking and post-masking.
(c) Differentiate between lossy and lossless compression techniques?
(d) Describe LBG algorithm to design codebook in a vector quantizer? Compare
date distortion performance of scalar and vector quantizers.

4. (a) With the help of block diagram, describe the working of a Code Exited LPC
(CELP) encoder. What is the role of perceptual weighting filter in it? Discuss
the bit allocation in 4.8 kbps (frame duration=30 msec) CELP speech coder.
(b) Draw the block diagram of a typical subband coder. Explain the roles of up-
sampling and down-sampling, analysis and synthesis filters in it. Derive the
conditions for perfect reconstruction for two band subband coder.

5. (a) What is the relationship between DCT and DFT? Is DCT the real part of
DFT? Justify your answer mathematically.
(b) Draw the block diagram of JPEG encoder and decoder and explain the role of
each block in encoder.
(c) Explain the suitability of wavelet transform for time-frequency analysis. How
it differs from STFT? Starting from 1-D continuous wavelet transform, derive
the expression of 1-D discrete wavelet transform.

6. (a) What do you mean by scalability in image coding? Give at least four features
of JPEG2000 that was not available in JPEG image coder.
(b) Why zig-zag scanning is used in JPEG image coder? How it helps in
improving the compression efficiency?
(c) The quantizers used in JPEG image coder take into account the characteristics
of human visual system up to some extent. Justify this statement.
(d) Why JPEG2000 performs basic coding on code blocks? Explain the difference
between Tier-I and Tier-II coding in JPEG2000.

7. Write short notes on any three of the following:
(a) Vector quantization
(b) SPIHT image coder
(c) Low Delay Code Exited Linear Prediction (LD-CELP) Speech Coder
(d) JPEG2000 Image Coder
1a) What is beyond 3G (B3G) wireless system? Make a comparison among 2G, 3G and B3G wireless systems on the basis of quality of service, roaming and types of switching.

1b) What do you mean by minimum noise factor $F_{\text{min}}$. The relationship between reflection coefficient $\Gamma$ and admittance $Y$ is given by following relation:

$$\Gamma = 1 - Y/1 + Y$$

Using the above relation, recast the equation for $F_{\text{min}}$.

$$F_{\text{min}} = 1 + 2R_* [G_{\text{opt}} + G_c]$$

in terms of real and imaginary parts of the reflection coefficient $\Gamma$. Where $R_*$ = noise resistance, $G_{\text{opt}}$ = optimum conductance and $G_c$ = correlation conductance.

1c) Make a comparison between deep sub-micron CMOS and HEMT device technologies for RF. Explain why HEMT technology has better noise performance.

2a) Write short-notes on the followings:
   i) Hetero-junction Bipolar Transistors (HBTs)
   ii) Wideband CDMA

2b) Derive an expression for input impedance $Z_{\text{in}}$ for the circuit of Fig. 1, by including MOSFET $M_1$ drain-to-source resistance $r_{ds}$, gate-to-drain capacitance $C_{gd}$ and gate-to-source capacitance $C_{gs}$ and trans-conductance $g_m$. Determine the value of inductance $L$, which makes the real part of $Z_{\text{in}}$ equal to zero.

![Fig. 1](image-url)

3a) Make a comparison between single gate and multiple gates silicon-on-insulator (SOI) MOSFETs. Explain which technology is better for scaling the device length in...
3b) What are the advantages of monolithic microwave integrated circuits (MMICs) over discrete circuits? List the basic characteristics required for an ideal substrate.

3c) Why scattering (S) parameters are used for RF/Microwave device characterization? Calculate the $S_{21}$ parameter for the circuit shown in Fig. 2.

![Fig. 2](image)

4a) Enumerate various steps involved in the design of power amplifier (PA). Design a class E power amplifier to deliver 1.5 W of power into 50Ω. Given that the supply voltage $V_{DD} = 3.3$ V and quality factor $Q = 20$.

4b) Carry out Z-parameters analysis of the transistor model given in Fig. 3 to show that:

$$
(Z_{11} - Z_{12})' = \frac{1}{R_b} \left( \frac{C_{rc} + C_{jc}}{C}_{rc} \right) + j\omega C_{jc}
$$

![Fig. 3](image)

4c) Differentiate between third generation 3G and fourth generation 4G wireless systems. What are the device and technology requirement for implementation of such type of systems?

5a) Differentiate between unity gain frequency $f_r$ and maximum frequency of oscillation $f_{max}$. Show that for deep sub-micron MOSFET (operating under high field region) $f_r$ is given by:

$$f_r = \frac{v_{sat}}{2\pi L}$$

Where $v_{sat}$ is saturation velocity and $L$ is the gate length of the MOSFET.

5b) Give brief answer to the followings:

(i) What are the important applications of Microwaves? Discuss.
(ii) Why PA used for PCS communication is mostly operated in class AB mode? Explain.
(iii) Differentiate between strip-line and micro-strip lines. Which is the more

Contd.............3
6a) i) If the gate-to-source overdrive voltages of a long-channel NMOS transistor is held at 1V, then what is the percentage change in the device transconductance as the temperature increases from 300K to 400K? Assume that mobilities of electron decreases by a factor of 2 as the temperature is increased.

ii) Calculate the noise figure of a receiver system shown in Fig. 4. Each block noise figure is denoted by F and corresponding power gain is denoted by G.

6b) Write short notes on the following:

(i) Drain induced barrier lowering (DIBL)
(ii) Back gate effect

7a) With help of a flow chart, explain various steps involved in the design of RF circuits. Briefly discuss their design goals and objectives.

7b) Carry out y-parameters analysis of circuit shown in Fig. 5 to show that

\[ C_n = \frac{\text{Im}(Y_n)}{\omega} - g_m \left( C_{gs} + C_{cb} \right) - C_{cb} \]

7c) Differentiate between the power match and the noise match. Explain why it is not possible to achieve both type of match simultaneously in a low noise amplifier.
1. (a) Distinguish between physical address, logical address, and port address. (5)

(b) Explain why a computer network based on a simple repeater hub is referred to as 'physically a star network, but logically a bus network'. (5)

(c) Distinguish between 10Base2, 10Base5 and 10BaseT forms of standard Ethernet. (5)

2. (a) The header and trailer in a Ethernet frame contains bits that are not part of user data and therefore constitute an overhead. What is the minimum and maximum value of this overhead expressed as a percentage of total frame length of IEEE802.3/Ethernet frame? The 8-byte preamble may be ignored in the calculations. (5)

(b) Consider building a CSMA/CD network running at 1 Gbps over a 1 km cable with no repeaters. The signal speed in the cable is 200,000 km/sec. What is the minimum frame size? (5)

(c) An IP packet is 60 bytes long including all its headers and it is to be transmitted on an Ethernet. If Logical Link Control (LLC) is not in use, is padding needed in an Ethernet frame, and if so, how many bytes? (5)

3. (a) Give suitable flow-charts showing the working of CSMA/CD medium access control for frame transmission. (5)

(b) What are the advantages offered by bridges over repeaters? (5)

(c) Distinguish between the signaling schemes used in 100Base-T4 and 100Base-TX. (5)

4. (a) Describe briefly the standards available for Gigabit Ethernet. (5)

(b) Describe why the MAC layer design of wireless LANs has to be different from that of wired ethernet? (5)

(c) Distinguish between the physical layer of IEEE802.11 a, b, and g standards? (5)
5. (a) Distinguish between hidden station problem and exposed station problem encountered in Wireless networks.

(b) Describe briefly the three power classes in the Bluetooth standard?

(c) Most Bluetooth devices operate at a transmission rate of 1 Mbps, but the actual throughput obtained is much lower. Give reasons for this.

6. (a) With regard to Bluetooth, (i) distinguish between SCO and ACL type of links, (ii) distinguish between piconet and scatternet.

(b) What is the difference between connectionless service and connection oriented service, with regard to Network layer operations in Wide Area Networks.

(c) What is Dijkstra’s Shortest Path algorithm?

7. Write short notes on any THREE of the following:
   (i) Distance Vector routing
   (ii) Hierarchical routing
   (iii) Multicast routing
   (iv) Flooding
   (v) Routing for mobile hosts
   (vi) Congestion Control