B. TECH. (AUTUMN SEMESTER) EXAMINATION  
(ELECTRONICS ENGINEERING)  
COMPUTER ARCHITECTURE  
CO-460

Maximum Marks: 60  
Credits: 04  
Duration: Two Hours

Answer all questions.  
Assume suitable data if missing.  
Notations and symbols used have their usual meaning.

<table>
<thead>
<tr>
<th>Q.No.</th>
<th>Question</th>
<th>CO</th>
<th>M.M.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1(a)</td>
<td>List various modes of transfer between Memory and I/O devices? Discuss in detail the DMA mode of transfer in a computer system with suitable diagrams.</td>
<td>(CO1)</td>
<td>[07]</td>
</tr>
<tr>
<td>1(b)</td>
<td>Discuss the Direct Mapping technique for cache memory. If the size of one block is 4 KB and the tag directory size is $10 \times 2^{12}$ bits, find the size of the main memory, cache memory and the tag bits for direct mapping.</td>
<td>(CO2)</td>
<td>[08]</td>
</tr>
<tr>
<td>1(b')</td>
<td>Discuss the Set-Associative Mapping for cache memory. If the size of one block is 4 KB and the tag directory size is $10 \times 2^{14}$ bits, find the size of the main memory, cache memory and the tag bits for a 4-way set-associative mapping.</td>
<td>(CO2)</td>
<td>[08]</td>
</tr>
</tbody>
</table>
| 2(a)  | Draw a block diagram for the hardware implementation of the following two statements:  

\[
x + yz : AR \leftarrow AR + BR  
x' + yz : AR \leftarrow AR + 1
\]

where, AR and BR are two n-bit registers and x, y and z are control variables. Include the logic gates for the control function. | (CO3) | [06] |
| 2(b)  | Discuss Instruction cycle using a flowchart. Also assume that an output program resides in memory starting from address 2300. It is executed after |

\[2\]
the computer recognizes an interrupt when FGO = 1 (while IEN=1).

a) What instruction must be placed at address 1? Explain.

b) What must be the last two instructions of the output program? Explain.

OR

2(b') List of register transfer language statements that change the content of accumulator are shown in Table 1.

<table>
<thead>
<tr>
<th>Control Function</th>
<th>Register Transfer Statement</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0T5</td>
<td>AC ← AC ∨ DR</td>
</tr>
<tr>
<td>D1T5</td>
<td>AC ← AC + DR</td>
</tr>
<tr>
<td>D2T5</td>
<td>AC ← DR</td>
</tr>
<tr>
<td>PB11</td>
<td>AC(0-7) ← INPR</td>
</tr>
<tr>
<td>RB11</td>
<td>AC ← AC'</td>
</tr>
<tr>
<td>RB9</td>
<td>AC ← shr AC, AC(15) ← E</td>
</tr>
<tr>
<td>RB7</td>
<td>AC ← shl AC, AC(0) ← E</td>
</tr>
<tr>
<td>RB6</td>
<td>AC ← 0</td>
</tr>
<tr>
<td>RB5</td>
<td>AC ← AC + 1</td>
</tr>
</tbody>
</table>

Table 1

Draw a gate structure for controlling the Load, Increment and Clear input of a 4-bit Accumulator.

3(a) The bits of microinstructions are divided into fields. Draw a hardware implementation to show the decoding of microoperation fields by Control Unit.

3(b) Discuss major characteristics of CISC and RISC architecture.

OR

3(b') Write Push and Pop microoperation for both Memory Stack and Register Stack. Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operation for evaluating the numerical result.

\[ (3 + 4) \times [10 + (2 + 6) + 8] \]
4(a) Define Parallel Processing. What is Temporal Parallelism? Derive an expression for speedup due to pipeline processing.

4(b) What do you mean by Interprocessor Arbitration? Discuss Serial Arbitration and Parallel Arbitration.

4(c) Find a routing path from PE2 to PE5 in 3-cube interconnection network, shown in Fig 1. Show each step very clearly.
2018-19
B.TECH (AUTUMN) SEMESTER EXAMINATION
(ELECTRONICS ENGINEERING)
DIGITAL IC DESIGN
(EL-413)

Maximum Marks: 60 Credits: 04 Duration: Two Hours

Answer all the questions.
Assume suitable data if missing.
Assume $V_{th}=0.43V$, $V_{tp}=-0.4V$, $V_{DSAT}=0.63V$, $V_{DSATP}=-1V$, $K_n=115E-6A/V^2$,
$K_p=-30E-6A/V^2$, $\lambda_n=0.06/V$, $\lambda_p=-0.1/V$

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<td>1(a)</td>
<td>How is it possible to reduce dynamic and leakage power of a digital circuit?</td>
<td>[04] CO1</td>
</tr>
<tr>
<td>1(b)</td>
<td>What is velocity saturation in a MOSFET? How does it affect the performance?</td>
<td>[04] CO1</td>
</tr>
<tr>
<td></td>
<td>OR</td>
<td></td>
</tr>
<tr>
<td>1'(b)</td>
<td>What is body effect? How can it be used to reduce static power consumption in CMOS?</td>
<td>[04] CO1</td>
</tr>
<tr>
<td>1(c)</td>
<td>Draw the layout of a Boolean function $Y=(A+BC)$ in static CMOS after sizing the transistors properly.</td>
<td>[07] CO1</td>
</tr>
<tr>
<td></td>
<td>OR</td>
<td></td>
</tr>
<tr>
<td>1'(c)</td>
<td>Draw the layout of a Boolean function $Y=(AB+CD+AD)'$ in static CMOS after proper sizing of transistors.</td>
<td>[07] CO1</td>
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<tr>
<td>2(a)</td>
<td>Design a combinational static CMOS circuit with proper sizing for 0.25u technology that implements $Y'=((A+B)(C+D+E)+F)G$. Also find out the worst and the best case input combinations for minimum $t_{pH}$ and $t_{PLH}$.</td>
<td>[06] CO1, CO2</td>
</tr>
<tr>
<td>2(b)</td>
<td>Draw the circuit of a full adder using minimum number of transmission gates and inverters. Explain briefly its realization.</td>
<td>[04] CO1, CO2</td>
</tr>
<tr>
<td>2(c)</td>
<td>What is logical effort 'g' and intrinsic delay 'p'? Compute the minimum delay of a 5 input NOR gate driving 5 identical NOR gates with respect to that of an inverter. Also compute the value of minimum delay.</td>
<td>[05] CO1, CO2</td>
</tr>
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<td>3(a)</td>
<td>Optimize the circuit, shown in Fig.1, for minimum delay along the path AB. Determine the sizes of different gates (Y and Z) and minimum delay.</td>
<td>[05] CO1, CO2</td>
</tr>
<tr>
<td></td>
<td>OR</td>
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Conf...
3'(a) Optimize the same circuit for minimum delay along the path AB by replacing NAND gates with NOR gates. Determine the sizes of different gates and minimum delay.

3(b) What is charge sharing problem in dynamic CMOS and how can it be solved? Also find the value of the minimum switching threshold voltage of an inverter which is being driven by a dynamic 6 input NAND gate. Assume that the value of its load capacitance is 10 times the individual node capacitances.

3'(b) Find the safe value of switching threshold voltage of the inverter which is being driven by a dynamic sum output of an adder. Assume that the value of its load capacitance is 4 times the individual internal node capacitances.

3'(c) Implement a full adder using np-CMOS logic

OR

3'(c) Implement a full adder using Domino logic

4(a) How is the C^2MOS register immune to 0-0 and 1-1 clock overlap? Compute the setup time of a static TG based flip-flop after drawing it circuit.

4(b) Describe briefly the design flow of a digital circuit with the help of a block diagram

4(c) Determine the transistor sizes of the clocked CMOS SR latch with an extra Enable signal for proper operation. Assume standard sizes for 0.25u technology of transistors for maximum speed for the regenerative inverter pair.

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Fig. 1

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Maximum Marks: 60  
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*Answer all questions.*  
*Assume suitable data if missing.*  
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| 1(a) | Describe briefly with suitable examples -  
   i. Activation Function in Artificial Neural Networks  
   ii. An Intelligent Agent                                      | (CO1) | [4] |
| 1(b) | Find if the following statement is a contradiction, a tautology or a satisfiable non tautology: \(((P\Rightarrow Q) \land (Q\Rightarrow P)) \iff (P\iff Q)\) | (CO1) | [4] |
| 2.   | Given that Ontable(A) \land Ontable(B) \land (Green(A) \lor Green(B)), using resolution in predicate logic show that \(\exists x (Ontable(x) \land Green(x))\). | (CO3) | [12] |
| 2'.  | Given the assertions.  
   A1: If a perfect square is divisible by a prime p, it is also divisible by square of p.  
   A2: Every perfect square is divisible by some prime.  
   A3: 225 is a perfect square.  
   A4: There exists a prime q such that square of q divides 225.  
   Show that A4 is logically implied by A1, A2, A3 using resolution in predicate logic. | (CO3) | [12] |
| 3.   | What is genetic algorithm? Give the flowchart of genetic algorithm. Describe in brief the different operators in genetic algorithm, with the help of examples. | (CO2) | [12] |
| 4.   | Implement the 3 variable logic function \(F = \sum(0, 2, 3, 6)\) using a multilayer perceptron network. | (CO4) | [12] |

*OR*

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<td>4'.</td>
<td>Design a Radial basis Function Network for strict interpolation of the given input-output pairs ({x_i, d_i} : {[0, 2], [1, -1], [3, 0]}).</td>
<td>(CO4)</td>
<td>[12]</td>
</tr>
<tr>
<td>5(a)</td>
<td>Describe how ANN can be used for localisation in wireless networks.</td>
<td>(CO5)</td>
<td>[06]</td>
</tr>
<tr>
<td>5(b)</td>
<td>Describe how ANN can be used for detection of heart diseases using ECG signals.</td>
<td>(CO5)</td>
<td>[06]</td>
</tr>
</tbody>
</table>
Answer all questions.
Assume suitable data if missing.
Notations and symbols used have their usual meaning.

Q.No. Question CO M.M.
1(a) List the critical issues and challenges for designing a multimedia communication system. (CO1) [03]
1(b) With the help of suitable block diagram of a multimedia communication system, discuss the basic components and requirements of a multimedia communication system. (CO1) [04]
1(c) What is the importance of Quality of Service (QoS) parameters in a multimedia communication system? Identify and explain the key QoS parameters associated with circuit-switched and packet-switched networks. (CO1) [04]
1(d) A multimedia Web-page of 10 MB is being retrieved from a Web server. Assuming a fixed delay of 5 msec within the server and trunk network, calculate and compare the total delay required to transfer the page over following access circuit:
   (i) A PSTN modem operating at 32 kbps.
   (ii) A high-speed modem operating at 8 Mbps.

2(a) With the help of suitable examples and diagrams, explain the sibling properties and tree-update rules for construction of a binary tree in adaptive Huffman Coding. (CO2) [05]

OR

2(a') Write the pseudo codes of adaptive Huffman encoding and decoding algorithms. (CO2) [05]
2(b) Name two LZ77-based Unix commands used for a file compression. Consider a text string ‘cabracadabrarrarrad’. Generate LZ77 encoded triplets using sliding window approach with window size=13 and search buffer size=07. Assuming the fixed length coding for each element of triplet codes, estimate the size (in bits) of compressed bitstream and compare it with uncompressed file size (with 7 bit ASCII code).

OR

2(b') Suppose the DCT coefficient matrix for a 4x4 image block is as shown below (dctblock). Use the procedures used in JPEG coder to:

(i) Quantize its DCT coefficients using the quantization matrix Q given below. Determine the value of quantized coefficients.

(ii) Arrange the quantized coefficients in zig-zag order and represent them as series of symbols using the runs of zeros. That is, generate a series of symbols, the first being the quantized DC index, the following symbols each consisting of a length of zeros and the following non-zero index, the last symbol is EOB (end of block).

\[
\textit{dctblock} = \begin{bmatrix}
31.00 & 51.70 & 1.17 & -24.58 \\
135.58 & 6.97 & -13.90 & 43.20 \\
195.58 & 10.14 & -8.67 & -2.94 \\
35.87 & -24.30 & -15.58 & -20.79
\end{bmatrix},
\]

\[
\textit{Q} = \begin{bmatrix}
16 & 11 & 10 & 16 \\
12 & 12 & 14 & 19 \\
14 & 13 & 16 & 24 \\
14 & 17 & 22 & 29
\end{bmatrix}
\]

2(c) Answer any two of the following questions.

(i) What is the role of zig-zag scanning of AC coefficients in JPEG image coder?

(ii) Why blocking artefacts are observed in very low bit-rate coded JPEG images?

(iii) How SNR scalability is achieved in JPEG 2000 image coder?

(iv) Name the entropy coding algorithm used in JPEG 2000 image coder. Why it is applied in two passes (Tier 1 and Tier 2)?
3(a) Assume an audio signal is divided into 16 frequency bands with energy in different bands as follows:

<table>
<thead>
<tr>
<th>Band</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level (dB)</td>
<td>0</td>
<td>8</td>
<td>12</td>
<td>10</td>
<td>6</td>
<td>2</td>
<td>10</td>
<td>60</td>
<td>35</td>
<td>20</td>
<td>15</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Assume that if the level of the 8th band is 60dB, it gives a masking of 12 dB in the 7th band, 15dB in the 9th band. How many bits you would need to code the 7th band and 9th band respectively? Suppose original signal is represented with 8 bits/sample/band.

OR

3(a') Explain why predictive coding (DPCM) can reduce the average bit rate compared to PCM coding of samples? Explain the principle of ADPCM and two different types of adaptation (forward and backward) and what are their pros and cons.

3(b) The linear predictive coding (LPC) is widely used for low bit-rate speech coding. Discuss the fundamental principles of LPC coders. Name the different variants of LPC coders. Give the distribution of bits among various parameters (on per frame basis) in LPC-10 coder and calculate the bit-rate.

OR

3(b') Explain the process of block motion estimation (BME) used in video coders. What is the role of search window in motion estimation? How the accuracy of motion vectors is improved in modern video coding standards?

3(c) List major differences between H.261 and H.263 video coding standard, between MPEG-1 and MPEG-2 standards (video part only), and between H.261 and MPEG-1 video coding standards. The differences may be in video formats that can be handled, the motion estimation methods, the use of deblocking filtering, the prediction methods, the intended applications, etc.

OR
3(c') A digitized CIF 4:2:0, 25 frames/sec video is to be compressed using MPEG-1 standard. Assuming a frame sequence of IPPPPPBBPPPBBPI... Differentiate clearly among I-, P- and B-frames. What are the implications of transmitting the compressed frames in this sequence? Also list the advantages and disadvantages of using B-frames.

4(a) What are the fundamental differences between multimedia downloading and multimedia streaming? Justify your answer. How the effects of network delay and jitter are compensated in real-time multimedia streaming?

4(b) What is the role of RTP in real-time multimedia communication? Explain its functionalities.

OR

4'(b) Name the ITU standard used in the end systems that supports multimedia communication over ISDN. Describe the audio and video coding procedure used in this standard.

4(c) What do you mean by Internet telephony or Voice-over-IP (VoIP)? Discuss the network requirements for following three possible scenarios of VoIP: PC to PC, PC to phone and phone to phone.