2015-16
B.TECH. (AUTUMN SEMESTER) EXAMINATION
ELECTRONICS ENGINEERING
COMPUTER ARCHITECTURE
CO-460

Maximum Marks: 60
Credits: 04
Duration: Three Hours

Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.

Q.No.  Question  M.M.
1(a)  What are Content Addressable Memories (CAM)? Why are they potentially faster [07]
than the Random Access Memories? What are the CAMs used for? Explain.
1(b)  With the help of suitable examples, differentiate between the memory-mapped I/O [08]
and I/O-mapped I/O.

OR

1'(a)  With the help of a suitable example, describe the mapping process in the segmented- [07]
paged memory management unit.
1'(b)  For a 16-bit addressing space with address duplication in place for the I/O mode, [08]
design an 8-bit input port that gets memory-mapped at hexadecimal address 6A6A.

2(a)  How can we realize the following logic functions using a full adder? Explain. [07]

<table>
<thead>
<tr>
<th>Control Signals</th>
<th>Required Logic Operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>s_2   s_1   s_0</td>
<td>OR</td>
</tr>
<tr>
<td>1     0     0</td>
<td></td>
</tr>
<tr>
<td>1     0     1</td>
<td>XOR</td>
</tr>
<tr>
<td>1     1     0</td>
<td>AND</td>
</tr>
<tr>
<td>1     1     1</td>
<td>NOT</td>
</tr>
</tbody>
</table>

2(b)  Find out the control words for the following Microoperations. Also, specify the [08]
functions being carried out by each of these Microoperations.

(i) R1 ← clc(R2 + R3 + 1)
(ii) R4-R2
(iii) Output ← shr(R4-R1-1)
(iv) R6 ← Input
(v) R2 ← R4 + 1
(vi) R7 ← R1-R4+1
(vii) R3 ← 0
(viii) R1 ← R4, C ← 1

OR

2' Design a 4-bit accumulator for the following microoperations: [15]

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Name of the Microoperation</th>
</tr>
</thead>
<tbody>
<tr>
<td>(i)</td>
<td>Add</td>
</tr>
<tr>
<td>(ii)</td>
<td>Clear</td>
</tr>
<tr>
<td>(iii)</td>
<td>Complement</td>
</tr>
<tr>
<td>(iv)</td>
<td>AND</td>
</tr>
<tr>
<td>(v)</td>
<td>OR</td>
</tr>
<tr>
<td>(vi)</td>
<td>XOR</td>
</tr>
<tr>
<td>(vii)</td>
<td>Shift-right</td>
</tr>
<tr>
<td>(viii)</td>
<td>Shift-left</td>
</tr>
<tr>
<td>(ix)</td>
<td>Increment</td>
</tr>
<tr>
<td>(x)</td>
<td>Check for Zero</td>
</tr>
</tbody>
</table>

3(a) With the help of a suitable block diagram, describe the functioning of a generic Microprogram Control Unit having a Control Memory of size 64×26. [07]

3(b) Using a minimum number of T-Flip-Flops, design the Hard-Wired Control for the addition and subtraction of two fixed-point binary numbers represented in sign-magnitude form. [08]

4(a) What do we mean by cache coherence? How can that be achieved in a multiprocessor environment? [07]

4(b) What is Merging? Discuss the Parallel Merging Algorithm. Find out the speed up achieved in Parallel Merging. [08]
2014-15
B.TECH. (AUTUMN SEMESTER) EXAMINATION
ELECTRONICS ENGG.
ANALOG IC DESIGN
EL 412

Maximum Marks: 60
Credits: 04
Duration: Three Hours

Answer all the questions.
Assume suitable data if missing.
Supplement you answers with neat circuit/block diagrams, wherever necessary.

Q.No. Question M.M. [04]
1(a) Figure 1 shows distribution of a reference for biasing in a large analog chip. What are the associated problems in the scheme; how can these be overcome?

![Figure 1]

1(b) Figure 2 shows a typical mixed signal circuit. What are the problems associated in its layout; and how can these be overcome?

![Figure 2]

Contd....2.
1(c) With the help of an example, explain "substrate coupling" and ways to overcome it.

1(d) Discuss possible implementations of integrated CMOS capacitors.

2(a) Find the small signal voltage gain and the -3dB frequency (in Hz.) for the active loaded (M2) inverting amplifier (M1), if (W/L)1=2μm/1μm; if (W/L)2=1μm/1μm. Assume dc current as 50μA, Cgd1=4fF, Cbd1=10fF, Cgd2=4fF, Cbd2=10fF, Cgs=5fF and C1=1pF. Also given: |V_T|= 0.7V, K'_{n}=2.2K'_{p}.

2(b) For the circuit as shown in figure 3, prove that the differential voltage gain is (4/3)g_{nn}R_{D}. Assume that the bias values of both V_{in1} and V_{in2} are equal.

![Circuit Diagram](image)

Figure 3

2' Analyze the circuit shown in figure 4 for the small signal voltage gain. Also identify the parasitic capacitances in the circuit. Find the expressions for unity gain frequency, bandwidth and slew rate.
3(a) How are switched capacitor circuits different from continuous time analog circuits? Realize a non-inverting switched capacitor amplifier circuit.

OR

3(a') Write brief technical note on FPAAs.

3(b) Explain the realization of a switched capacitor unity gain sampler circuit.

3(c) Obtain the switched capacitor realization of the circuit shown in figure 5 and discuss its design considerations.

4(a) How is analog IC design different from discrete design?

4(b) How do parasitic capacitances affect the performance of a MOS switch?

4(c) Design a two MOS transistors based voltage controlled active resistor.

4(d) Design a two MOS transistor based voltage reference circuit.

4(e) How can a current amplifier be realized using two MOS transistor? Derive its small signal gain, input and output resistances.
2015-16
B.TECH. (AUTUMN) VII SEMESTER EXAMINATION
(ELECTRONICS ENGINEERING)
DIGITAL IC DESIGN
(EL-413/EL-413N)

Maximum Marks: 60
Credits: 04
Duration: Three Hours

Answer all the questions.
Assume suitable data if missing.

Assume \( V_{tn}=0.43 \text{V}, V_{tp}=-0.4 \text{V}, V_{DSATn}=0.63 \text{V}, V_{DSATp}=-1 \text{V}, Kp'=115E-6 \text{A/V}^2 \cdot Kp''=-30E-6 \text{A/V}^2, \lambda_n=0.06 \text{V/V}, \lambda_p=-0.1 \text{V/V} \)

Q.No.  

1(a) What is the importance of subthreshold slope? How can it be reduced?  
1(b) Why is the interconnect delay crucial at the nanoscale? Justify.  
1(c) What is meant by velocity saturation? How does it affect the drain current?  
1(d) Draw the layout of an XOR gate after sizing it properly.  

OR

1′(d) Draw the layout of an XNOR gate after sizing it properly.  

2(a) What is the voltage swing on the output node in Fig. 1? Estimate the energy drawn from the supply for a 0V to 2.5V transition at the input. Compute \( V_{OH} \)  
2(b) Compute \( V_{OH}, V_{OL} \) and \( V_{M} \) of the circuit shown in Fig. 2  
2(c) Determine the sizes of additional two buffers in the chain to obtain the minimum delay in the circuit shown in Fig. 3. Also compute the value of the minimum delay.  

3(a) What are the problems associated with dynamic logic and pass transistor logic? Which logic will most likely dominate at the nanoscale and Why?  

OR

3′(a) Optimize the circuit, shown in Fig. 4, for minimum delay along the path AB. Determine the delay and the sizes of different gates. Repeat the problem after replacing NAND gates by OR gates.  

3(b) What is the importance of logical effort 'g' and intrinsic delay 'p' in combinational gates? Determine the value of 'g' and 'p' for an XNOR gate.  

Contd.....2.
after drawing its circuit.

3'(b) Find the safe value of switching threshold voltage of the inverter which is being driven by a three input dynamic NAND gate. Assume that the value of its load capacitance is 15 times the individual internal node capacitance.

3(c) Implement the full adder using Domino logic

OR

3'(c) Implement the full adder using np-CMOS logic

3(d) For the level restorer shown in Fig. 5, assume that the pull down device consists of two pass transistors with a device size of 0.5u/0.25u replacing the transistor Mn. Determine the maximum W/L size for the level restorer transistor for correct functionality. Assume that the inverter has a switching threshold equal to V_{DD}/2.

OR

3'(d) Implement the carry of the full adder using static CMOS by properly sizing the transistors? What are the input patterns that give worst case tPLH and tPHL by considering the capacitance of the input nodes? Justify your answer.

4(a) Describe the parameters on which the clock frequency of a sequential circuit depend.

4(b) Discuss the design of a C^2MOS register? How is this circuit immune to clock overlap?

OR

4'(b) What is the importance of pipelining in a sequential system? Why is it preferred over parallel processing?

4(c) An Enable signal has to be inserted in a ratioed but unclocked CMOS SR latch such that the latch functions only when Enable = 1. Determine the transistor sizes of the unclocked CMOS SR latch with Enable signal for proper operation. Assume standard sizes for 0.25u technology of transistors forming the regenerative inverter pair with V_{M}=V_{DD}/2.

4(d) What is the significance of setup time and hold time in the design of sequential system?

OR

4'(d) Compute the setup time and clock to Q delay of a static transmission gate based master/slave negative edge triggered FF. What is the problem with this circuit? What is the assumption made before computing these delays.
Fig. 1

Fig. 2

Fig. 3

Fig. 4
1(a) With the help of suitable diagrams, clearly differentiate between 7-layered OSI protocol and TCP/IP protocol.

OR

1(a') (i) In an OSI layered framework, define protocol and service. Explain their differences.
(ii) What is the difference between a physical address and a network address?
(iii) Suppose a machine is attached to several physical networks. Why does it need a different IP address for each attachment?
(iv) Explain why framing information is required even in case where frames are of constant length.

1(b) Suppose a TCP entity receives a digital voice stream from the application layer. The voice stream arrives at a rate of 8000 bytes/sec. Suppose TCP arranges bytes into block sizes that result in a total TCP and IP overhead of 50%. How much delay is incurred by the first payload byte in each block (of length L bytes)? Assume zero processing delay.

OR

1(b') Suppose a header consists of four 16-bit words: (11111111 11111111, 11111111 00000000, 11110000 11110000, 11000000 11000000). Find the Internet checksum for this code.
1(c) Two computers are connected by an intercontinental link with a one-way propagation delay of 100 msec. The computers exchange 1-Megabyte files that they need delivered in 250 ms or less. The transmission lines have a speed of R Mbps and the bit error rate is $10^{-8}$. Design a transmission system by selecting the bit rate R, the ARQ protocol, and the frame size (assume that the overhead $n_o = 64$ bits).

**OR**

1(c') Derive the expression for transmission efficiency of selective repeat request protocol.

2(a) The Ethernet standard specifies a minimum MAC frame size (there is a pad field in the 802.3 MAC frame to achieve this minimum size if the packet is too short). This is necessary because a node may not detect a possible collision before it completes its transmission of a very short packet. In a maximum size 10BaseT (10-Mbps, baseband, twist-pair) Ethernet, the longest propagation delay (including repeater delays) is 51.2 $\mu$s. The propagation speed in copper is approximately $2 \times 10^8$ m/s. Find the minimum frame size.

2(b) Let G be the total rate at which frames are transmitted in a slotted ALOHA system. What proportion of slots go empty when the system is operating at its maximum throughput?

2(c) Compare FDMA, TDMA and CDMA in terms of their ability to handle group of stations that produce information at constant but different bit-rates.

**OR**

2'(a) Derive the expression for maximum throughput in slotted ALOHA system. Clearly state any assumptions made.

2'(b) Calculate the normalized delay-bandwidth product (parameter ‘a’) and maximum throughput for a Gigabit Ethernet switch with stations at 100-meter distance and average frame size of 512 bytes and 1500 bytes.

2'(c) Use IEEE 802.3 and IEEE 802.11 to discuss three differences between wired and wireless LANs.

Contd.....3.
3(a) Name some metrics that can be used to assign cost to links, for finding shortest path between source and destination nodes in a network.

3(b) Explain the advantages of hierarchical routing over flat routing. Also differentiate between routing tables in packet-switched network and datagram network.

3(c) For the network shown in Figure below, use Bellman-Ford algorithm to find the set of shortest paths from node 4 to other nodes. Find the set of associated routing table entries.

4(a) Identify the range of IPv4 addresses spanned by class A, class B, class C and class D addressing schemes.

OR

4(a') Abbreviate the following IPv6 addresses:

   (i) 0000:0000: 0000:0000:0000:0000:0000:004D:ABCD
   (ii) 2819:00AF:0000:0000:0000:0035:0CB2:B271

4(b) Perform CIDR aggregation on the following /24 IP addresses: 128.56.24.0/24; 128.56.25.0/24; 128.56.26.0/24; 128.56.27.0/24.

4(c) Suppose a packet arrives at a router and is to be forwarded to an X.25 network having an MTU of 576 bytes. The packet has an IP header of 20 bytes and a data barts of 1484 bytes. Perform fragmentation and show the fragments that router creates and specify the relevant values in each fragment header (i.e. total length, fragment offset and more bits).

4(d) What approach is used to interconnect islands of IPv6 networks separated by IPv4 networks? Explain the process of interconnection.
2015-16
B.TECH. (AUTUMN SEMESTER) EXAMINATION
ELECTRONICS ENGINEERING
ARTIFICIAL INTELLIGENCE AND NEURAL NETWORKS
EL-432N

Maximum Marks: 60 Credits: 04 Duration: Three Hours

Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.

Q.No. | Question | M.M.
---|---|---
1(a) | Solve the 5-queens problem using an incremental formulation with a suitable search algorithm. | [05]
1(b) | Give the properties of the task environment for chess playing agent, taxi driving agent and part picking robot. | [06]
1(c) | Compare the Space and Time complexity of Depth First Search and Bidirectional Search for the following data.
Branching factor = 4, maximum depth = 10, depth of Goal = 5, space required = 1000 bytes/ node and speed = 1000 nodes/ second. | [04]
2(a) | Represent the following sentences in Conjunctive Normal Form (CNF) for First Order Logic.
R1: Everyone who loves all animals is loved by someone.
R2: Anyone who kills an animal is loved by no one.
R3: Jack loves all animals.
R4: Either Jack or Curiosity killed the cat, who is named Tuna. | [08]
2(b) | How PROLOG is different from Standard First Order Logic? Give one example of a sentence written in PROLOG. | [03]
2(c) | What is Logical Equivalence? Write the following Logical Equivalences in the form of expressions:
Double-Negation Elimination, Contraposition, Implication Elimination and | [04]

Contd...2.
Biconditional Elimination.

OR

2'(a) Represent the following sentences in First Order Predicate Logic (FOPL):  [08]
R1: Horses, cows and cats are mammals.
R2: An offspring of a horse is a horse.
R3: Bluebeard is a horse.
R4: Bluebeard is Charlie’s Parent.
R5: Offspring and Parent are inverse relations.
R6: Every mammal has Parent.

From this Knowledge Base (KB) prove that Offspring of Bluebeard is Charlie and Charlie is a mammal using Forward Chaining Algorithm.
2'(b) Write all the de Morgan Rules for quantified sentences.  [02]
2'(c) What are different types of logical connectives used in Propostional Logic? Explain. Also give the truth table of each logical connective.  [05]

3(a) Give the diagram of Biological Neuron and its mathematical model along with the various activation functions that are commonly used.
3(b) What are different types of learning techniques associated with artificial neural networks? Explain Hebbian Learning. Design a Hebbian Learning based neural network for 2 input XOR function with bipolar inputs and targets.
3(c) Design a Radial Basis Function (RBF) network to implement XNOR function using \( \sigma = 1/\sqrt{2} \).

OR

3'(a) Implement the 3 variable logic function \( F = \sum (0, 2, 3, 6) \) using minimum number of McCulloch Pitts Neurons.
3'(b) What are Feedback neural networks? Explain Discrete Hopfield Network along with its architecture.
3'(c) What is a linearly separable function? How many neurons are required to implement a linearly separable function of 10 inputs? Implement a Majority function of 5 inputs.

4(a) Design a neural network to classify the input patterns according to the classes
4(b) What is the role of Artificial Neural Networks (ANN) in the field of Robotics and Communication?
Maximum Marks: 60  
Credits: 04  
Duration: Three Hours

Answer all the questions. Each question is of 15 marks. 
Assume suitable data if missing. Notations used have their usual meaning.

Q.No.  
Question  
M.M.

1(a) Describe briefly the following terms: Morphing, Superimposition, and Digital Recasting.  
[5]

1(b) With regard to a multimedia presentation, enumerate the strengths and weaknesses of each of the following media elements (i) text (ii) video.  
[5]

1(c) With regard to performance of voice recognition systems, distinguish between Insertion error and Substitution error. 

OR

1'(c) Write a short note on recent trends in flat panel displays.  
[5]

2(a) What is Unicode standard? Describe the usefulness of this standard in modern day communications.  
[5]

2(b) Taking the help of a suitable example, explain briefly the basic principles of Arithmetic coding.  
[5]

OR

2'(b) What are the psycho–visual redundancies in an image that can be exploited in the compression of a still image to be viewed by a human eye?  
[5]

2(e) Describe briefly those features of JPEG-2000 which distinguishes it from JPEG.  
[5]

Contd.....
3(a) Write a short note on classification of microphones.

3(b) What is perceptual audio coding? Are there any standards which utilize this?

OR

3(b') A studio quality digital video system is to be designed using 4:2:2 sampling format for acquiring CCIR601 format from a PAL YUV signal having 625 lines/frame and 25 frames/second. Calculate the number of samples per line for (i) the luminance signal, (ii) each of the two chrominance signals. Assume that the entire video signal (including blanking periods) is to be encoded.

3(c) Describe briefly those features of MPEG-4 video which distinguishes it from MPEG-1 and MPEG-2 video.

4(a) Explain briefly the significance of timing relationships in networked multimedia.

4(b) Distinguish between packetizing delay, transmission delay, and propagation delay in a networked environment.

OR

4(b') Explain briefly the mechanisms used for achieving Synchronization Accuracy Specification (SAS) limits.

4(c) With regard to HTML, what is the significance of (i) Head, (ii) Body, and (iii) Title.
### Question 1

A. Explain the interlaced scanning. What are its advantages? 

OR

A'. Describe the two photovoltaic effects used for converting variations of light intensity into electrical signals.

B. Define vertical and horizontal resolution.

C. Why maximum video frequency is 5 MHz in India?

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### Question 2

A. What is HDTV? Explain why it has an increased aspect ratio over regular TV.

OR

A'. Explain suitability of transmitting R-Y & B-Y colour difference signals.

B. What is DBS? What are the signal frequencies and levels used? Why RF and IF signal processing is done prior to the MPEG-2 decoding?

C. Discuss the relative merits and demerits of the three television colour systems. Why the colour burst signal is transmitted after each scanning line?
| Q3 | A. Assuming $R$ is the maximum unambiguous range of a low PRF radar, calculate the ratio of the signal strength for a target at $(\frac{3}{4})R$ and $(\frac{5}{4})R$. If a target with a radar cross section of 20 m² exists at $(3/4)R$, what should the target cross section be at $(5/4)R$ to result in an equal signal strength at radar?

B. By what factors pulse repetition frequency is governed? What is meant by ambiguous range?  

OR

B’ Explain the effects of various parameters on radar range equation. |
|---|---|
| Q4 | A. What is the cause of Doppler shift? How large is it for typical radar frequencies and targets? What is the sign of the change it causes when the target and radar are closing on each other??  

OR

A. What is the basic structure of a radar receiver? Explain how AFC is achieved in the radar receiver.

B. Compare the A scope and PPI radar display, by stating the advantages and applications of each.  

OR

B’. The noise figure of a radar receiver is 12dB and its bandwidth is 2.5Mhz, what is the value of minimum receivable power?

C. If two MTI radars operate at the same PRF of 2 kHz with different operating frequencies, then find the ratio of the operating frequencies. Assume the second blind speed of one radar is 5 times blind speed of the second. |