2013-14
B.TECH. AUTUMN (VII SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
COMPUTER ARCHITECTURE
CO-460

Maximum Marks: 60
Credits: 04
Duration: Three Hours

Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.

Q. No.  Question                                                                                              Marks

1(a)  Discuss the DMA transfer in computer system with suitable diagram.                           [06]
1(b)  What is an associative memory? Discuss its hardware organization and match logic. [06]

OR

1(b') Discuss locality of reference in cache memory. What are different types of mapping procedures in cache memory? Discuss any two in detail. [06]

1(c)  i. How many 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes? [03]
     ii. How many lines of address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all RAM chips?
     iii. How many lines must be decoded for chip select? Specify the size of the decoders.

2(a)  i. Design an arithmetic circuit with two selection variables S1 and S0 and two 4 bits data inputs A and B. The circuit generates the following arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram of 4 bit arithmetic circuit. [06]
     | S1 | S0 | C_{in}=0                                      | C_{in}=1                                      |
     |----|----|----------------------------------------------|----------------------------------------------|
     | 0  | 0  | A + B' (subtract with borrow)                | A + B' + 1 (Subtract)                        |
     | 0  | 1  | A (transfer A)                               | A + 1 (Increment A)                          |
     | 1  | 0  | A + B (Add)                                  | A + B + 1 (Add with Carry)                   |
     | 1  | 1  | A - 1 (Decrement A)                          | A (Transfer A)                               |

ii. Draw and explain the flow chart for complete computer operation. [06]

OR

Cmd......2
2(a)  
i. Write the register transfer statements for the fetch and decode phases of instruction cycle. How register transfer statement for fetch phase can be implemented in the bus system?  
ii. How does BSA (Branch and Save Return Address) work? Explain with suitable example. Write its microoperations.

2(b) Which of the following register transfer statements are wrong and why?  
i. \( xT: AR \leftarrow \overline{AR}, AR \leftarrow 0 \)  
ii. \( yT: R1 \leftarrow R2, R1 \leftarrow R3 \)  
iii. \( zT: PC \leftarrow AR, PC \leftarrow PC+1 \)  

3(a) How micro-program sequencer works in micro-programmed control unit? Explain with suitable diagram. Give the input logic truth table for microprogram sequencer.

OR

3(a') In bus organization with CPU registers, how the following operation is performed?  
\( R1 \leftarrow R2 + R3 \)

3(b) What is the difference between hard-wired control and microprogram control? What are advantages and disadvantages in each method?

3(c) Write the microoperations for the push and pop for both Register Stack and Memory Stack.

4(a) What is pipelining? Explain with suitable example. Derive its speed-up formula.

4(b) What is interconnection structure? Write brief notes on the following  
i. Hypercube System  
ii. Multistage switching network

4(c) What is instruction pipeline? Draw the flowchart for 4-segment instruction pipeline.

OR

4(c') Differentiate between tightly coupled and loosely coupled multiprocessors.
2013-14
B.TECH. (AUTUMN SEMESTER) EXAMINATION
ELECTRONICS ENGG.
ANALOG IC DESIGN
COURSE CODE: EL-412

Maximum Marks: 60
Credits: 04
Duration: Three Hours

Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.
Supplement your answers with necessary circuit/block diagram.

Q. No.          Question                      M.M.

1(a) Comment on the graph as shown in Figure 1, formulate the plotted expression. [06]

MOS Switch ON Resistance as a Function of Gate-Source Voltage

![Graph Image]

Figure 1

1(b) Derive the expressions for gain and bandwidth of an active loaded inverting amplifier. [06]

1(c) Write a brief technical note on FPAAs. [3]

2(a) For the circuit of Figure 2, explain and analyse the same for the output resistance. [06]
Identify the circuit and its application(s) along with its limitation(s)

Contd......2
2(b) Design the circuit of Figure 3 for Slew Rate of 10V/us; if the circuit is to drive a 10pF load. What is the bandwidth of the circuit, if the transistors used have \( V_A = 30V \)? Also find the device aspect ratios, if a gain of 15 is desired.

2'(a) Explain the operation of the circuit of Figure 4 and design the circuit for an output current of 2 times the input current.

2'(b) Identify the various parasitic elements in the circuit of Figure 4 and comment qualitatively as well as quantitatively on their effects on the circuit's performance.
3(a) Design the circuit of Figure 5 for eliminating the systematic offset problem.

3(b) What are the advantages of employing a PMOS input stage in the design of a two-stage CMOS opamp?

OR

3(b') Show the systematic design of a Gilbert Cell.

3(c) Design a Switched-capacitor multiply by two circuit OR a switched-capacitor parasitic insensitive integrator circuit.

4(a) With the help of an example, explain the effect of Substrate Coupling in mixed signal circuits.

4(b) With the help of an example, explain the effect of capacitive coupling between interconnects in a mixed signal circuit.

4(c) How does differential signalling and shielding reduce crosstalk between signals?

4(d) How can the effects of linear gradients be suppressed in laying the differential pair transistors?
2013-14
B.TECH. (AUTUMN SEMESTER) EXAMINATION
ELECTRONICS ENGINEERING
DIGITAL IC DESIGN
EI-413N

Maximum Marks: 60 Credits: 04 Duration: Three Hours

Answer all the questions.
Assume \( V_{in} = 0.43V, \ V_{tp} = 0.4V, \ V_{pd} = 0.63V, \ V_{pd4} = -1V, \ K_n = 115E-6A/V^2, \ K_p = -30E-6A/V^2 \)
\( N_o = 0.00V, \ A = 0.1V \)
Notations used have their usual meaning.

Q No. | Question | M.M.
--- | --- | ---
1(a) | What is the importance of subthreshold region of operation of a MOS transistor? | 06
1(b) | What is subthreshold slope? How it can be reduced? | 04
1(c) | What is meant by velocity saturation? How does it affect the drain current? | 03
1(d) | What are the problems with CMOS technology? Which other devices have the potential to replace CMOS? | 05
2(a) | Calculate the switching threshold \( V_M \) of the inverter in Fig. 1 for \( V_{DD} = 0.35V \). | 06

OR

2'(a)(i) | What is the voltage swing on the output node in Fig. 2? | 02
2'(a)(ii) | Estimate the energy drawn from the supply for a 0V to 2.5V transition at the input. | 02
2'(a)(iii) | Compute \( V_{OH} \) | 02
2(b) | Determine \( t_{DL} \) and the output voltage in case of a circuit shown in Fig. 3, assuming a step input from 2.5 to 0V at the input. | 04
2(c) | Compute the expression of minimum delay through a chain of inverters to derive a high capacitive fanout load. | 05

OR

2'(c) | Determine the sizes of the additional two buffers in the chain to obtain the minimum delay in the circuit shown in Fig. 4. Also compute the value of the minimum delay. | 05
3(a) | Why the straightforward cascading of dynamic gates does not work? Explain briefly. | 02

Cond.....2
3(b) Optimize the circuit, shown in Fig. 3, for minimum delay along the path AB.

OR

3'(b)(i) What is the logic function implemented by the CMOS network in Fig. 6?

3'(b)(ii) Realize the NMOS and PMOS devices with NMOS W/L=4 and PMOS W/L=8.

3'(b)(iii) What are the input patterns that give worst case tPLH and tPHL by considering the capacitance of the input nodes? Justify your answer.

3(c) For the level restorer shown in Fig. 7, assume that the pull down device consists of three pass transistors with a device size of 0.5μ/0.25μ, replacing the transistor M1. Determine the maximum W/L size for the level restorer transistor for correct functionality. Assume that the inverter has a switching threshold equal to VDD/2.

OR

3'(c)(i) Explain that the circuit shown in Fig. 8, consumes static power consumption.

3'(c)(ii) How can the static power consumption be reduced by the insertion of an additional transistor? Also size that extra transistor.

3(d) What is the advantage and disadvantage of PTL over static CMOS?

OR

3'(d) Which is the most popular logic style and Why?

4(a) Explain the different parameters on which the clock frequency of a sequential circuit depend.

4(b) Discuss the design of a C^2MOS register? How is this circuit immune to 0-0 and 1-1 clock overlap?

OR

4'(b) Compute the setup time and clock to Q delay of a static transmission gate based master-slave positive edge triggered register. What is the problem with this circuit?

4(c) It is required to insert an Enable signal in the ratioed clocked CMOS SR latch such that the latch functions only when Enable =1. Determine the transistor sizes of the latch with Enable signal for proper operation. Assume standard sizes for 0.25μ technology of transistors forming the regenerative inverter pair.

FIGURE ENCLOSED

Cond. ......3
Fig. 1

Fig. 2

Fig. 3

'1' is the minimum size inverter.

Fig. 4

Fig. 5

Contd.......

4
AUTUM SEMESTER B.TECH. EXAMINATION 2013-14
ELECTRONICS ENGINEERING
COMPUTER COMMUNICATION NETWORKS
EI-431N

Max. Marks: 60
Credits: 04
Time: Three Hours

Attempt All Questions
Symbols used carry their standard meaning.
Make suitable assumptions where necessary.

1. A telephone modem is used to connect a personal computer to a host computer. The speed of the modem is 56 kbps and the one-way propagation delay is 100 ms. Find the efficiency for Stop-and-Wait ARQ if the frame size is 256 byte. Assume a bit error rate of $10^{-5}$, zero processing delay, 64 bit acknowledgement and 64 bits for header and CRC.

1b. Suppose a large message having $10^5$ bits is to be transmitted over two hops. If the transmission line in each hop has an error rate of $10^{-5}$ and that each hop does error checking and retransmission. How many bits will be transmitted for a successful reception using message switching.

1c. Explain how bit stuffing is used in HDLC to avoid occurrence of flag inside the frame.

2a. Suppose that the ALOHA protocol is used to share a 56 kbps satellite channel. Suppose that frames are 1000 bits long. Find the maximum throughput of the system in frames/second.

2b. Explain how collision avoidance is achieved in a wireless communication network.

2c. What is collision domain? Explain how it can be reduced in a computer network.

OR

2a. Calculate the ring latency in terms of bits for a link speed of 4Mbps having 20 stations with an average inter-station separation of 100m. Assume the processing delay of 2.5 bits at each station.

2b. MAC can alternate between Contention Periods and Contention-Free Periods. Elaborate this statement.

2c. Prove that in a polling system using exhaustive service having $M$ stations with equal walk times of $t$ and frame transmission time $X$ is given by:

$$\text{Efficiency} = \frac{MX - Mt}{T_e}, \text{where } T_e \text{ is average cycle time}$$

Contd………2
3a Explain with example how the problem of Counting-to-Infinity is solved.

3b Suppose that ATM cells arrive at a leaky bucket policer at times $t = 1, 2, 3, 5, 6, 8, 11, 12, 13, 15$, and $19$. Assuming the increment per arrival equal to 4 and the bucket depth as 10, plot the bucket content and identify any nonconforming cells. What will be the effect if the depth of the bucket is increased?

OR

3' a In a computer communication network a message of duration $T$ seconds is split into $k$ packets of equal length. If the communication between source and destination requires $L$ hops, find the minimum delay after which the entire message is received at the destination. Calculate the saving in time if cut through switching is employed.

3' b A sub-network shown in Figure 1 uses the Bellman-Ford algorithm for routing packets in the network. Given the cost of each link in the sub-network, find the routing Table assuming Node 6 as the destination.

![Figure 1: Sub-network using Bellman-Ford algorithm](image)

4a Explain how two level and three level of hierarchy is introduced in IPv4.

4b Given the address comment on the validity of the address, IP version of the protocol used and give the expanded hexadecimal address.
   a) 4DF5:0A5F:39A:A:2176
   b) ::FFFF:128.155.12.298

4c An IP header is shown in the figure below. Calculate the value in the checksum field.
Maximum Marks: 60

Question

1(a) What are the different types of search techniques used in artificial intelligence? [5]

1(b) If the branching factor is 8 and maximum depth of the tree is 150, then find out the storage usage in breadth first search (BFS) and depth first search (DFS) techniques. Assume the goal node to be at maximum depth and the storage available is 100 bytes/node. [5]

1(c) Describe the local search technique in brief. What are its main advantages? [5]

(OR)

1'(a) What are the various steps required to be performed by problem solving agents? Explain them in brief. [5]

1'(b) What is iterative deepening first (IDF) search? Explain by taking a suitable example. [6]

1'(c) What do you understand by simulated annealing search? [4]

2(a) Explain the following terms in brief:
   i) Semantics
   ii) Entailment
   iii) Inference
   [9]

2(b) What are different types of sentences used in first order predicate logic (FOPL)? [3]

2(c) What are the special features of PROLOG? [3]

3(a) Give a mathematical model of a neuron. [4]

3(b) What are different types of learning techniques associated with artificial neural networks? Explain any two of them. [8]

3(c) Design an artificial neural network for 'OR' operation using threshold function. [3]

4 Explain in detail any two of the following applications of artificial neural network (ANN) in the followings areas:
   i) Bioinformatics
   ii) Forecasting
   iii) Intrusion Detection
   iv) Communication [15]
B.TECH. (AUTUMN SEMESTER) EXAMINATION  
ELECTRONICS ENGINEERING  
MULTIMEDIA SYSTEMS AND NETWORKS  
EI-447

Maximum Marks: 60  
Credits: 04  
Duration: Three Hours

Answer all the questions. Each question is of 15 marks. 
Assume suitable data if missing. 
Notations used have their usual meaning.

Q.No.  

1(a) What is the meaning of the term 'hyphen'? Does this have any relevance to multimedia?  

1(b) What are the advantages of electronic pen over mouse and keyboard?  

1(c) Write a brief note on the competing technologies for flat panel displays.  

OR

1'(c) What are the measures used to determine voice recognition performance?  

2(a) With the help of a suitable example, explain briefly the basic principles of Arithmetic coding.  

OR

2'(a) Briefly discuss the advantages of LZW coding over LZ coding.  

2(b) Distinguish between bitmap and vector representation of images.  

OR

2'(b) Why is Group 4 two-dimensional compression standard considered less robust as compared to Group 3 two-dimensional compression standard?  

2(c) Which part(s) of JPEG encoder is/are typically responsible for information loss, and why?  

Contd........2
3(a) Describe briefly what is meant by perceptual audio coding?

3(b) An NTSC encoded video clip has frame size of 720 x 480 pixels and is digitized using 8 bits for each of Y, Cb, and Cr and a chroma sub-sampling scheme of 4:2:2. Calculate the file size of 1 minute of video clip and the total time taken for it to be transmitted over a 2 Mbps link.

3(c) For a video consisting of a sequence of I-frames, P-frames, and B-frames:
(i) define the term Prediction span (generally denoted by M)
(ii) define the term Group of pictures (generally denoted by N)
(iii) determine the values of M and N for the sequence IBPBBPBPBB1...

OR

3'(c) A digitized video is to be compressed using the MPEG-1 standard. Assuming a frame sequence of IBPBBPBPBB1..., and average compression ratios of 10:1 for I-frames, 20:1 for P-frames, and 50:1 for B-frames, derive the average bit rate that is generated by the encoder for the PAL digitization format.

4(a) Describe briefly the Synchronization Accuracy Specification (SAS) factors used in networked multimedia.

4(b) Distinguish between jitter and skew in networked multimedia. How can they be minimized?

OR

4'(b) With regard to multimedia network, enumerate the factors that contribute to delay.

4(c) Distinguish between minimum buffer strategy and maximum buffer strategy in a networked multimedia environment.
Q. No.             Question                                                                                                        M.M.

1(a)             Find the minimum reuse distance and user capacity (no. of users per cell) for a TDMA cellular system with hexagonally shaped cells, path loss exponent $n = 2$ for all signal propagation in the system, and BPSK modulation. Assume an AWGN channel with required SIR = 5 dB, a total system bandwidth of $B = 50$ MHz, and a required signal bandwidth of 100 KHz for each user. [04]

1(b)             A mobile terminal samples signals from four BSs as a function of time. The times and received signal strengths (in dBm) from the samples are given as:

<table>
<thead>
<tr>
<th>Time (s)</th>
<th>0</th>
<th>2.5</th>
<th>5</th>
<th>7.5</th>
<th>10</th>
<th>12.5</th>
<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td>BS$_1$</td>
<td>-47</td>
<td>-57</td>
<td>-52</td>
<td>-55</td>
<td>-60</td>
<td>-62</td>
<td>-60</td>
</tr>
<tr>
<td>BS$_2$</td>
<td>-59</td>
<td>-56</td>
<td>-55</td>
<td>-54</td>
<td>-52</td>
<td>-51</td>
<td>-49</td>
</tr>
<tr>
<td>BS$_3$</td>
<td>-70</td>
<td>-72</td>
<td>-75</td>
<td>-70</td>
<td>-58</td>
<td>-50</td>
<td>-61</td>
</tr>
<tr>
<td>BS$_4$</td>
<td>-72</td>
<td>-71</td>
<td>-65</td>
<td>-60</td>
<td>-55</td>
<td>-53</td>
<td>-50</td>
</tr>
</tbody>
</table>

Assume that the mobile is initially attached to BS$_1$. The mobile makes handoff decisions by considering the signals from the BSs after each sampling time. Write down the handoff transitions between BSs for each of the following algorithms at each of the sampling time. If a condition is met for more than one BS, assume the best one (strongest RSS) is selected.

a. RSS
b. RSS + threshold of -60 dBm
c. RSS + hysteresis of 10 dB

1(c)             Differentiate between multipath and shadow fading. Give an example distribution that is used to model these fading. [05]

OR

1(c')            A mobile system is to provide 95 percent successful communication at the fringe of

Contd......2
coverage with a shadow fading component having a zero mean Gaussian distribution with standard deviation of 8 dB. What fade margin is required?

2(a) Differentiate between flat and frequency selective fading, fast and slow fading. What are parameters used to characterize them?

2(b) Consider a single branch Rayleigh fading signal has a 20% chance of being 5 dB below some mean SNR threshold. Find the probability that a 3-branch selection diversity receiver will be 6 dB below the mean SNR threshold.

2(c) Discuss how using cycle prefix and IDFT/DFT, OFDM decomposes a frequency selective-fading channel into a set of N parallel flat-fading channels.

OR

2'(a) For a Rayleigh faded envelope, find the percentage of time that a signal is 10 dB or more below the RMS value.

2'(b) Determine the average probability of bit error for DPSK signal in a flat Rayleigh fading channel.

2'(c) Discuss briefly the advantages and disadvantages of CDMA access techniques for mobile system.

3 (a) Discuss how a 13 kbps speech signal in GSM system is channel coded to 22.8 kbps.

3(b) Discuss how variable spreading factor (VSF) is used to provide variable bit rate (VBR) traffic in a CDMA system.

3(c) Why is new infrastructure needed for GPRS? Which component is new and what is their purpose?

4(a) Discuss briefly the physical layer characteristics of 3G system based on WCDMA.

OR

4(a') Discuss briefly some key characteristics that distinguish 3G mobile systems from 2G mobile systems.

4(b) Discuss briefly different parameters that define the MAC layer priorities in IEEE 802.11 WLAN

4(c) Discuss how RTS (request to send) and CTS (clear to send) controls packets are used for contention-free access in IEEE 802.11 standard.