1. (a) Explain Data transfer from I/O device to CPU in Programmed I/O mode with suitable block diagram.

(b) What do you mean by the concept of Virtual Memory? Write short notes on address space and memory space.

(c) A computer employs RAM chips of 256 X 8 and ROM chips of 1024 X 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers. (i) How many RAM and ROM chips are needed? (ii) Draw a memory-address map for the system. (iii) Give the address range in hexadecimal for RAM, ROM, and interface.

2. (a) Draw one stage of bus line with three state-buffers. Explain how many decoders and three state-buffers are needed to design a bus system for k registers of n bits each to produce an n-line common bus.

(b) How can you design a binary decremener ($A \leftarrow A - 1$)? Justify your answer. Design a 4-bit combinational circuit decremener.

(c) The 8-bit registers $AR$, $BR$, $CR$, and $DR$ initially have the following values:

\[
AR = 11110010 \\
BR = 11111111 \\
CR = 10111001 \\
DR = 11101010
\]

Determine the 8-bit values in each register after the execution of the following sequence of microoperations:

\[
AR \leftarrow AR + BR \\
CR \leftarrow CR \land DR, BR \leftarrow BR + 1 \\
AR \leftarrow AR - CR
\]

OR
2. (a) Consider the initial configuration of 4096 X 16 Memory as shown in Fig. 1. Initially the content in AC is 456 (in hex), and after fetch and decode phase the content of PC is 21. AC and PC both are 16-bit registers. After execution phase what will be the content of accumulator register AC.

\[
\begin{array}{|c|c|c|}
\hline
20 & 1 & ADD \\ 
21 & 1 & AND \\ 
22 & 0 & CMA \\ 
\hline
123 & & \\ 
124 & & \\ 
\hline
\end{array}
\]

Fig. 1

(b) Draw the flowchart for the interrupt cycle. Write the condition/Register transfer statement for setting the value of interrupt register to 1.

(c) Write the register transfer statements for the fetch and decode phases of the instruction cycle.

3. (a) Define the following: (i) microoperation, (ii) microinstruction, (iii) microprogram and (iv) microcode.

OR

(a') Write down the major characteristics of RISC and CISC architecture.

(b) (i) Explain how the mapping from an instruction code to a microinstruction address can be done by means of a read-only memory.

(ii) Write the microoperations for the push and pop operations for Register Stack.

(c) A computer has 16 registers, an ALU with 32 operations, and a shifter with eight operations, all connected to a common bus system. (i) Formulate a control word for a microoperation. (ii) Specify the number of bits in each field of the control word and give general encoding scheme. (iii) Show the bits of the control word that specify the microoperation \( R4 \leftarrow R5 + R6 \).

4. (a) Draw a suitable diagram of a pipeline unit for floating-point addition and subtraction.

OR

(a') Draw a suitable diagram of an X 8 omega switching network and determine how many stages and switches are needed in an n X n omega switching network.

(b) Draw a diagram showing the structure of a four-dimensional hypercube interconnection network. List all the paths available from node 7 to node 9 that use the minimum number of intermediate nodes.
Considering \((W/L)\) as the design parameter, answer the following with justifications:

(i) How can the resistance of an analog MOS-switch be reduced to half?
(ii) How can the MOS-switch sampling speed be doubled?
(iii) Design a PMOS loaded CS amplifier for a gain of 5.
(iv) How can the resistance of a diode connected MOS transistor be doubled?
(v) Design a single-ended input current amplifier for a gain of 5, keeping in view the matching and symmetry considerations.

\[5 \times 3\]

2. Analyze an active loaded \((M2: \text{PMOS})\) inverting amplifier \((M1: \text{NMOS})\) for small signal gain, output resistance and bandwidth. What value of \(V_{in}\) will yield a current of 100 microamperes if \((W/L)_1 = 5\), \((W/L)_2 = 2\). For this value of \(V_{in}\), find the small signal gain and output resistance assuming transistors in saturation region.

\[15\]

OR

2'. For an active loaded \((\text{PMOS})\) differential amplifier \((\text{NMOS})\), derive the expressions for small signal voltage gain, output resistance and lower 3dB frequency. Also find slew rate and ICMR. Now answer the following questions:

(i) Does output resistance depend on constant current source value?
(ii) Which transistor(s) aspect ratio affect upper ICMR and lower ICMR?
(iii) Which transistor(s) aspect ratio decide the gain of the amplifier?
(iv) What is the trade-off in gain and bandwidth?

\[15\]

3.(a) Identify the effective parasitic capacitances in the circuit shown in figure-1 and hence find the circuit’s time constant, assuming a clock frequency \(f_c\).

\[03\]

(b) What are PCAs and PRAs and how are these actually implemented?

\[03\]

(c) Justify the utility of figure-2 as a CAD for FPAA application by showing at least nine different functionalities.

\[09\]

OR

\[2\]
(c') Explain the function performed by the circuit shown in figure-3 and rename A, B and C according to functionality and conventional notations. Also suggest design modifications if (i) the output resistance looking into 'C' is to be increased, (ii) Channel length modulation induced errors (in M₁⁻ and M₂⁻) are to be overcome.

4. (a) What is the significance of multi-finger transistors?
(b) What is common centroid layout technique?
(c) What are the major steps in analog IC design process?
(d) Discuss some applications of Gilbert cell.
(e) What are the problems of laying a CS stage close to a NAND gate?
2012-2013
B.TECH. AUTUMN (VII SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
DIGITAL INTEGRATED CIRCUIT DESIGN
(P1L-413 N)
Credits: 04

Maximum Marks: 60

Answer all questions.

1.(a) Give the description of the fixed cost and variable cost of Integrated Circuits. 04

OR

(a') What is meant by the 'performance' of digital integrated circuits? What are the factors on which it depends and how it is commonly measured? 04

(b) Discuss use of Copper and low-K dielectrics in integrated circuits. 03

OR

(b') Discuss three dimensional ICs. 03

(c) Obtain equivalent resistance of a MOSFET while (dis)charging a capacitor. Also explain some important conclusions from the expression of the equivalent resistance. 08

2.(a) Discuss in detail the modelling of parasitic capacitances in ICs. What happens when thickness of wire strip becomes comparable or more than its width and when there are more number of layers of wire forming interlayer capacitance? 08

(b) Discuss 'salicide', 'polyicide' and 'current crowding' for the strips of the connecting wires in integrated circuits. 05

OR

(b') Derive the expression of the minimum delay in a chain of CMOS inverters. 05

(c) Obtain the sizes of the PMOS and NMOS transistors such that the switching threshold of a CMOS inverter, implemented in 0.25 μm process, is located at 1.5V. Supply voltage being 2.5 V and assume suitable values for the parameters. 04

(c') Find all the values of the capacitance linearization factor $K_{eq}$ for the high-to-low transition case in a CMOS inverter with $\phi_0=0.8$ and $m=0.5$ and 0.44 for the bottom plate and side walls, respectively. 04

3.(a) How the propagation of complimentary CMOS gates (say NAND /NOR) is evaluated? How it depends on the input signal pattern? 06
(b) Explain optimization of the performance in combinational networks through 'electrical' and 'logical efforts'.

OR

(b') Describe important characteristics of mirror adder. Sketch is not necessary.
(c) Describe level restoration in a pass-transistor logic design including the sizing of the level restorer transistors.

OR

(e') Explain 'charge leakage' and 'charge sharing' in dynamic circuit design.

4.(a) Sketch a reduced clock load static master-slave register using multiplexers. Show its problems during operation including effect of non-ideal clock signals.

OR

(a') Discuss driving off-chip capacitances and the advantages of using progressively-sized inverter chain.
(b) Discuss (1-1) overlap in a CMOS master-slave positive edge triggered register.
(c) Sketch a specialized truly single-phase edge-triggered register.
1a. Show that if the generator polynomial in a cyclic code has more than one term and the coefficient of $x^n$ is 1, all single errors in the code word can be successfully detected.

1b. Explain with the help of diagram why and how limits are set on transmit and receive window size in Selective Repeat ARQ.

1c. In a Network with one Primary A and two Secondaries B and C, polling is used employing Normal Response Mode HDLC. Explain the NRM in HDLC and the sequence of communication between Primary and Secondaries as shown in Figure 1.

The symbol ‘X’ shown in Figure 1 indicates an error during transmission.

![Diagram of communication between Primary A and two Secondaries B and C polling using Normal Response Mode HDLC.]

2a. Suppose that 80 percent of the traffic generated in the LAN is for stations in the LAN, and 20 percent is for stations outside the LAN. Is an Ethernet Hub preferable to an Ethernet switch? Does the answer change if the percentages are reversed?
2 b Discuss different Token Reinsertion Policies in a Ring topology. If a network has normalized ring latency of 10, suggest a Token Reinsertion algorithm to be used with proper justification.

2 c In a CSMA/CD protocol, prove that:

\[ \text{Average Contention Period} = 2t_{\text{prop}} + e \text{ seconds} \]

where \( t_{\text{prop}} \) is the propagation delay and \( e = 2.718 \).

OR

2'a Differentiate between Physical and Virtual Carrier Sensing used in IEEE 802.11.

2'b What is hidden terminal problem in a wireless LAN? Explain how it is solved.

2'c Discuss different classification of reservation schemes used for medium access in a computer network.

3 a With reference to routing, state the Optimality Principle. For the sub-network shown in Figure 2 draw the sink tree for node 4.

3 b In a computer network a complete message can be transmitted by a source in 2 ms duration. If the message reaches the destination in 5 hops and each hop has 10 μs propagation delay, calculate:

i) the time required to receive the message at the destination.
ii) the time required to receive the message at the destination if message is split into 10 equal size packets.
iii) the time required to receive the message at the destination (as in ii) if cut through packet switching is used.

OR

3' a Differentiate between Open Loop and Close Loop Congestion Control Algorithms.
A sub-network shown in Figure 2 uses the Shortest Path Dijkstra's algorithm for routing packets in the network. Given the cost of each link in the sub-network, find the Routing Table assuming Node 6 as the source.

Figure 2: Sub-network using Shortest Path Dijkstra's algorithm

4 a  What are the advantages of having Classless Addressing in a Computer Network? Differentiate between subnetting and super networking.

4 b  Given the address 132.6.17.85, find the network class, network address, netid and hostid. Find also the maximum number of hosts that can be connected to this network.

4 c  Draw the TCP/IP protocol suite and show how the encapsulation process is carried out.
2012-13
B. Tech. Autumn (VII Semester) Examination
(Electronics Engineering)
Multimedia Systems and Networks (EL-447)

Maximum Marks: 60
Credits: 04
Time: 3 hours

Any missing data can be suitably assumed. Symbols used have their standard meanings.

1 (a) Describe briefly the following terms: Morphing, Superimposition, and Digital Recasting.

(b) With regard to preparation of a multimedia presentation, enumerate the strengths and weaknesses of each of the following media elements: (i) text (ii) video.

(c) Discuss briefly the multimedia applications in the area of health and medicine.

OR

(c') Describe briefly the various steps involved in recognition of cursive handwriting?

2 (a) With the help of a suitable example, explain briefly the basic principles of Arithmetic coding.

(b) (i) The LZ algorithm is to be used to compress a text file. If the average number of characters per word is 7, and the dictionary used contains 4096 words, derive the average compression ratio that is achieved relative to using 7-bit ASCII codewords.

(ii) A GIF image occupies a rectangular area of A inch by B inch on a monitor screen. The resolution of the monitor is C dpi. What is the file size of the image in KBytes?

(c) Using suitable block diagram(s), explain briefly the working of JPEG encoder / decoder.

OR

(c') Enumerate the differences between JPEG and JPEG2000.

3 (a) Write a short note on classification of microphones.

OR

(a') An input signal has a flat frequency spectrum in the range 0 to W Hz, and the signal does not have any frequency present outside this range. Do you think sub-band coding implementation for this signal can achieve compression? Why?

(b) Distinguish between temporal masking and frequency masking.

(c) A studio quality digital video system is to be designed using 4:2:2 sampling format for acquiring CCIR601 format from a PAL. YUV signal having 625 lines/frame and 25 frames/second. Calculate the number of samples per line for (i) the luminance signal, (ii) each of the two chrominance signals. Assume that the entire video signal (including blanking periods) is to be encoded.

OR

(c') Distinguish between the characteristics of MPEG-1 video and MPEG-2 video.
4 (a) With regard to temporal relationships, briefly describe (i) object stream interactions, (ii) media levity, and (iii) media synchronization.

(b) Enumerate the factors that contribute to delay in a networked multimedia environment.

OR

(b') Distinguish between jitter and skew in networked multimedia. How can they be minimized?

(c) With regard to HTML, what is the significance of (i) Head, (ii) Body, and (iii) Title.
2012-2013

B. Tech Winter (VIII semester) Examination

(ELECTRONICS ENGINEERING)

TV & RADAR ENGINEERING – EL-458

Maximum Marks – 60       Credit–4       Duration --3 Hours

Q1 (a) Define the followings : (5 marks)

   i, brightness

   ii, Resolution

   iii, Luminance & Chrominance

Q1. (b) Calculate the sound and picture carrier frequency for channel 10(192-198MHz for NTSC system) before and after frequency translation to the IF frequency. What is the required local oscillator frequency? (5 marks)

   OR

Q1 (b') Calculate the increase in horizontal and vertical resolution if the video modulating signal frequency is increased to 20 MHz for NTSC. (5 marks)

Q1(c) Draw the composite video waveform at the end of either field, labeling all the pulses shown. (5 marks)

Q2 (a) In the (R-Y), (B-Y) color TV subcarrier demodulation system, (G-Y) signal is obtained from the (R-Y) & (B-Y) signals, that is

\[ m_c(t) - m_y(t) = K_2[m_u(t) - m_y(t)] + K_3[m_b(t) - m_y(t)] \]

   (a) Find the values for K_2 & K_3 that are required.

   (b) Draw a block diagram for a (R-Y), (B-Y) system and explain how it works. (5 marks)

Q2 (b) Explain, the choice of color subcarrier frequency in NTSC system. (5 marks)

   OR

Q2(b') Define the TV standards and compare their performance. (5 marks)

Q2(c) Describe the 4:2:2 formats used to digitize component video. (5 marks)
Q7(a') What is SDTV? Give a reason why it has a decreased aspect ratio over HDTV. (5 marks)

Q3 (a) A pulse radar transmits pulses whose pulse width is 1.2 micro seconds. The repetition rate of pulse is 0.8 KHz. Determine the maximum and minimum ranges of the radar. (5 marks)

OR

Q3(a') If the noise figure of a radar receiver is 2.5 dB, what reduction measured in dB occurs in the signal to noise ratio at the output compared to the signal to noise ratio at the input? (5 marks)

Q3(b) What is the peak pulse power of a radar pulse, if pulse width is 2 micro sec, the pulse repetition rate is 900 and the average power is 18 W. What is the duty cycle? (5 marks)

Q3(c) Discuss the various losses in radar systems. (5 marks)

Q4(a) Two MTI radars operate at different PRFs, PRF1 = 2*PRF2. They are operating at frequencies f1 & f2. If the 3rd blind speed of 1st is 4 times of 5th blind speed of 2nd, then find the ratio of the operating frequencies. (5 marks)

Q4(b) What is the difference between antenna scanning and tracking? Describe with help of block diagram the conical scan method of tracking an acquired target. (5 marks)

Q4(c) The azimuth angle of a target found from the PPI is 60 degree and the height of the target is 10 km. Find the range of the target from radar. (5 marks)

OR

Q4(c') Compare the A scope and PPI radar displays, by stating the advantages and applications of each. (5 marks)