2016-17
B.TECH. (AUTUMN SEMESTER) EXAMINATION
(ELECTRONICS ENGINEERING)
DIGITAL ELECTRONICS
(EL-311)

Maximum Marks: 60
Credits: 04
Duration: Two Hours

Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.

Q.No. Question M.M.
1(a) Explain the basic operation of Emitter Coupled Logic (ECL) circuit. Draw the
ECL circuit with addition of an emitter-follower. Also draw ECL OR/NOR
[08]
gate.

1(b) Sketch the circuits of
(i) TTL AND-OR-INVERT gate
[04]
(ii) open collector output (buffer/driver), which can drive high current/high
[03]
voltage load.

1' (b) Using appropriate values of components, analyse and explain the working of a
Tri-State TTL NAND gate. [07]

2(a) Give the advantages of BiCMOS logic circuit. Sketch and explain the most
[09]
improved version of Bi-CMOS inverter.

2(b) Using pass-transistor logic (PTL) and complementary pass-transistor logic
(CPL), implement the following functions
(a) OR-NOR
(b) XOR-XNOR

Contd... 2
3(a) Using circuit diagram, explain how data is written, read and erased in an EEPROM.

OR

3'(a) Using sense amplifier and equalization circuit, explain READ and WRITE operation of a SRAM cell.

3(b) Draw the complete Diagram to arrange several $2K \times 8$ PROM to produce a total capacity of $8K \times 8$. Give the address range of each PROM in Hexadecimal code.

4(a) Analyse and design the circuit of a 4-bit, R-2R Ladder DAC, that gives inverting output in the range 0-10V, having single pole double through switches between ground and virtual ground. Take Reference supply as 10 V.

4(b) Using appropriate circuit Analyse and explain the circuit of
   (a) Successive approximation ADC
   OR
   (a') Dual slope integrator ADC
Maximum Marks: 60  
Duration: Two Hours

Answer all the questions.  
Assume suitable data if missing. 
Notations used have their usual meaning.

Q.No.  

1(a) Draw and explain the frequency response of integrator. Also give its phase value.  
1(b) For a low pass notch filter shown in Fig. 1, \( \omega_n = 1 \text{rad/sec}, \ \omega_m = 1.2 \text{rad/sec}, \ Q = 10, \) and a dc gain of unity. Find the frequency and magnitude of the transmission peak. Also find the high frequency transmission.

![Diagram of integrator circuit](image)

Fig. 1

1'(a) What is the significance of filter parameter quality factor (Q)? Explain the effect on frequency response of high pass filter and low pass filter for \( Q > 1/\sqrt{2} \)

1'(b) Find the order required for a Chebyshev low pass filter whose requirements are characterized by \( A_{\text{max}} = 1 \text{dB}, \ A_{\text{min}} = 35 \text{dB}, \ f_p = 2000 \text{Hz}, \ f_s = 5000 \text{Hz}. \) Also determine the loss at 5000Hz.

[Cont'd... 2]
2(a) What is the frequency transformation technique? Also give its significance.

2(b) A low pass filter is required to meet the following specifications:
\[ A_{\text{max}} = 0.5 \text{dB} \quad A_{\text{min}} = 25 \text{dB} \quad f_0 = 1 \text{ KHz} \quad f_c = 3 \text{ KHz} \quad \text{dc gain} = 0 \text{dB} \]
Find the Chebyshev approximation function for these requirements and realize it using Saraga design

OR

2'(a) Describe the cascade approach for current mode circuits.

2'(b) Show the block diagram implementation of the following transfer function and realize the block diagram to obtain the Tow Thomas biquad. Design the circuit for \( K = 2 \), \( Q = 2 \) and \( \omega_o = 2 \text{Krad/sec} \), assuming capacitors of 1nF.

\[ \frac{V_o}{V_i} = \frac{-K}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \]

3(a) Realize the ideal grounded inductor using OTA and grounded capacitor. Also give the attractive features of the circuit realized.

3(b) Design Antoniou GIC based second order band pass filter with a centre frequency of 10 KHz, 3dB band width of 500Hz and a centre frequency gain of 10. Use \( C = 1.2 \text{nF} \).

4(a) What are the advantages of CCCII over CCII? Realize CCII-based and CCCII-based CM ideal grounded integrator which can be implemented in monolithic IC technology.

OR

4(c) What are the Quadrature Oscillators?

4(b) What are the Tuned Amplifiers? Draw and explain the circuit of Single-Tuned Amplifier and also give its applications.
Max. Marks: 60
Answer all questions. All symbols have their usual meaning in the context of this course.

Q.1.  (a) Write a Verilog description for gate level circuit of a 1-bit Full Adder. Using this 1-bit Full Adder module, write a Verilog code for 4-bit Ripple Carry Adder. (10)

(b) Describe the function of various Bitwise operators available in the Verilog HDL. (5)

(b') In the given block diagram, CLK to Q delay and Setup time for all the registers are 0.5ns and 1ns respectively. Delay of the adder and multiplier units are given to be 3 ns and 7 ns respectively. Assume wire delay to be 1ns. Find the maximum clock (CLK) frequency that can be used for this system while ensuring correct operation for all the paths. (5)

Q.2.  (a) Design an inverter chain, using the method of Logical Effort, to drive \( C_L = 256C_{in} \) with minimum delay. \( C_{in} \) is the input capacitance of the first stage inverter with \( W_P/W_N = \gamma \). (10)

(a') The given CS stage must achieve a voltage gain of 15 with a power budget of 0.9mW. Assuming \( \lambda_1 = 0.15V^{-1} \), \( \lambda_2 = 0.05V^{-1} \), \( \mu_pC_{ox} = 200 \mu A/V^2 \), \( \mu_nC_{ox} = 100 \mu A/V^2 \), and \( V_{TN} = |V_{TP}| = 0.4V \), determine the \( W/L \) for \( M_2 \). If \( M_1 \) is of same size as \( M_2 \), find the bias voltage \( V_b \). (10)

(b) Estimate the FO4 delay of a 3-input NAND gate. Assume that the NAND gate is matched to the reference inverter with \( W_P/W_N = 2 \). Take the value of \( \tau = 2ps \). (5)

Q.3.  (a) Write short notes on the following IC fabrication process steps: (10)

(i) Annealing, and (ii) Chemical Vapor Deposition.

(b) A silicon wafer with n-type background doping concentration of \( 2 \times 10^{16} \text{ cm}^{-3} \) is subjected to a boron implant with an implant energy of 80keV and implant dose of \( 10^{14} \text{ cm}^{-2} \). It is given that for this implant process \( R_p = 0.24 \mu \text{m} \) and \( \Delta R_p = 0.063 \mu \text{m} \).

(i) What is the depth of the peak of the implanted profile?

(ii) How much peak concentration of boron is achieved through this implant step?

(iii) What is the concentration of boron at the depth of 0.45 \( \mu \text{m} \)?
(b') Arsenic is diffused at 1100°C for 2hrs with an initial dose of $10^{14}$ cm$^{-2}$ to achieve a Gaussian doping profile. If the wafer had a p-type background doping concentration of $10^{17}$ cm$^{-3}$, find the surface concentration of As and junction depth at the end of diffusion process. The diffusivity of As at the given diffusion temperature is given to be $2\times10^{14}$ cm$^2$/s.

Q.4. (a) With the help of suitable diagram, describe major process steps involved in the fabrication of a typical BJT.
(b) Describe the Junction Isolation techniques in IC fabrication. Also list their advantages and disadvantages.

OR

(b') Describe Dielectric Isolation techniques in IC fabrication. Also list their advantages and disadvantages.
2016-17
B.TECH. (AUTUMN SEMESTER) EXAMINATION
ELECTRONICS ENGINEERING
MICROPROCESSORS AND MICROCONTROLLERS
EL-332

Maximum Marks: 60 Credits: 04 Duration: Two Hours

Answer all the questions.
Assume suitable data if missing. Question No 1 to 3 are related to 8085A and its related peripherals
Notations and symbols used have their usual meaning.

Q.No. Question M.M.
1(a) i) The Instruction group of the “LXI H, 2500H” is
A) Immediate B) Arithmetic [0.75]
C) Register Indirect D) Data transfer

ii) How many T-states are needed for the execution of XCHG Instruction?. [0.75]

iii) A certain instruction was executed in 8085 µP. The contents of the ACC before and after
execution were respectively 48H and 24H. Identify the Instruction.

iv) Draw the format of Flag register of 8085 µP. Give the importance of each of its flag
through appropriate Instruction [1.5]

[3.0]

1(b) i) Compare CALL and PUSH Instructions of 8085 µP. [3.0]

ii) Write a program using 8085 µP’s instructions for multiplying two numbers stored in
memory locations 2500H and 3500H using Shift and Add method. The result may be
stored at an address location of your choice

OR

ii’) Explain with the help of suitable timing diagram and flow chart the operation of
Interrupt Acknowledge machine cycle. [6.0]

2(a) i) How many hardware interrupts are available in 8085 µP? [1.0]

ii) Programmed data transfer is used
a) When relatively large data is transferred using relatively slower I/O devices
b) When small amount of data is transferred using relatively slower I/O devices [1.0]

c) When small amount of data is transferred using relatively faster I/O devices
d) None of the above is true

iii) Give a brief classification of various data transfer schemes. [3.0]

2(b) i) Differentiate between Synchronous and Asynchronous mode of Data transfer [3.0]
ii) A fast multiplier chip is to be interfaced with a microprocessor 8085. Draw a scheme of interfacing the above. Also give the program associated with it for loading the data in R1 and R2 registers and reading the multiplication data from R3 register. Assume the following (1) chip takes 300 ns for multiplication. (2) the chip has three registers for holding the two 8-bit operands and their product. (3) It has four different addresses associated with it along with a chip enable line. The multiplication starts as soon as the second operand is loaded in the Register R2.

OR

ii) Draw the functional block diagram of 8257 DMA controller chip. Explain the function of each block in it.

3(a) i) What is the addressing range of 8085 µP [1.0]
   a) 4096  b) 128 Kb  c) 256 Kb  d) 64 Kb
ii) 8255 PPI is an IC that is used for [1.0]
    a) For serial Data transfer  b) Input/ Output Interfacing
    c) providing timing signals  d) None of these is correct
iii) What is the need for Interfacing? Discuss in brief the incompatibilities present. [3.0]

3(b) i) What do you understand by address decoding? Explain with the help of suitable example. [3.0]
ii) A microprocessor based system is to be designed with the following hardware arrangement.

22K of RAM (RAM is available in block of 8K using 6264 chips and 2K using 6116 chips)
32 K of ROM (ROM is available in block of 8k through 2764 chips)

Four 8255's with address starting at F000H. Assume that 3X8 decoder, 2X4 decoder, 1X2 decoders along with other combinational gates are available to the designer. Draw

a) Memory map
b) Complete decoding scheme
c) Complete diagram of the realised system

OR [7.0]

ii) Draw the functional block diagram of 8253 programmable interval timer. With the help of neat timing diagrams explain various programming modes of 8253 Timer.
4(a)   i) Give the format of TCON register of 8051 µC. Explain the meaning of each bit in it.  [2.5]
    ii) Compare and contrast between 8085 µP and 8051 µC.  [3.0]

4(b)   i) Give the format of flag register of 8086 Microprocessor with suitable explanation of additional flags.  [3.5]
    ii) Draw the configurations of timer 0 in various modes. Explain each configuration.  [6.0]

OR

ii) In a microcontroller based system it is desired to generate a square wave of frequency 100 Hz at P1.1. Write a program for the above using timer 0 in mode 1. Assume the crystal frequency to be 11.0592 Mhz.
A sinusoidally modulated AM signal \( f(t) \) is applied to the square-law device, such that the output voltage \( e_0(t) \) is \( e_0(t) = [f(t)]^2 \). Show that the ratio of the second harmonic to the first harmonic in \( e_0(t) \) is equal to \( \mu/4 \).

Determine the instantaneous frequency of the signal \( g(t) \) which is given as:

\[
g(t) = \cos(200\pi t)\cos(5\sin(2\pi t)) + \sin(200\pi t)\sin(5\sin(2\pi t))
\]

OR

The single tone modulating signal \( m(t) = A_m\cos(2\pi f_m t) \) is used to generate the VSB signal

\[
s(t) = \frac{1}{2}aA_mA_c\cos[2\pi(f_c + f_m)t] + \frac{1}{2}A_mA_c(1-a)\cos[2\pi(f_c - f_m)t]
\]

where \( a \) is a constant, less than unity, representing the attenuation of the upper side frequency.

If we represent this VSB signal as a quadrature carrier multiplex

\[
s(t) = A_c m_1(t)\cos[2\pi f_c t] + A_c m_2(t)\sin[2\pi f_c t]
\]

Find out \( m_2(t) \)?

The VSB signal, plus the carrier \( A_c\cos(2\pi f_c t) \) is passed through an envelop detector. Determine the output of the detector and the distortion produced by the quadrature component.

\[\text{contd...}\]
1’ b Draw the block diagram of an AM Superheterodyne Radio Receiver and discuss the constraints imposed on the choice of Intermediate Frequency.

2 a State and explain sampling theorem for low pass signals.

2 b Draw a frame format of T1 system and calculate the bit rate and channel bandwidth required. Explain the use of elastic store with reference to the T1 system.

2 c Draw the block diagram of a DPCM system and explain its working.

3 a Explain a method by which the threshold effect in FM can be reduced.

3 b A signal can be modelled as a lowpass stationary process $X(t)$ whose PDF at any time $t_0$ is given in Figure 1. The bandwidth of this process is 5 kHz, and it is desired to transmit it using a PCM system.

i. If sampling is done at the Nyquist rate and a uniform quantizer with 32 levels is employed, what is the resulting SQNR?

ii. What is the resulting bit rate?

3’ b What are the different types of noise encountered in a communication system?

For a communication system using single tone Amplitude Modulation with full carrier, prove that the Figure of Merit of a receiver based on envelop detection is $1/3$.

4 In pulse transmission system using matched filter detection prove that the average probability of symbol error in a binary symmetric channel depends solely on the ratio of the transmitted signal energy per bit to the noise spectral density. Assume the pulse amplitude of $-A$ and $+A$ represents the two symbols 0 and 1.
Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.

Q. No. | Question                                                                                                                                                                                                 | M.M.
-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----
1      | In the Manchester code, binary symbol '1' and '0' are represented as follows: \[ s_1(t) = \begin{cases} 1 & 0 \leq t \leq T_b/2 \\ -1 & T_b/2 \leq t \leq T_b \end{cases} \text{ for '1'} \]
       | \[ s_2(t) = \begin{cases} -1 & 0 \leq t \leq T_b/2 \\ 1 & T_b/2 \leq t \leq T_b \end{cases} \text{ for '0'} \] Derive the formula for the probability of error incurred by the maximum likelihood detection procedure applied to this form of signaling over an AWGN channel. | 15  
2(a)  | Consider a 4-PSK constellation with \( d_{\text{min}} = \sqrt{2} \). What is the additional energy required to send one extra bit (8-PSK) while keeping the same minimum distance (and thus with the same bit error probability)? | 05  
2(b)  | Compare the bandwidth and power efficiency trade-offs of M-ary PSK and FSK modulations.                                                                                                                   | 05  
2(c)  | A 16-level QAM system transmits information at a rate equal to that achievable by a combination of two QPSK systems and an eight-level PSK system. Identify the signal constellation for these three PSK systems.                      | 05  

OR

2'. Consider the octal signal point constellation shown in Figure 1.
   i. The nearest signal points in the 8-QAM signal constellation are separated in distance by 'A' units. Determine the radii 'a' and 'b' of the inner and outer circles.
   ii. The adjacent signal points in 8-PSK are separated by a distance of 'A' units. Determine the radius 'r' of the circle. | 05  

contd... 2
iii. Determine the average transmitter powers for the two-signal constellation and compare the power advantage of one constellation over the other? (Assume that all signal points are equally probable.)

![Fig.1.

3(a). A binary source emits symbols \( x_1 \) and \( x_2 \) with probabilities 0.6 and 0.4, respectively. Design a Huffman code for the second order extension of the source and determine its code efficiency.

3(b). Consider a binary channel with channel matrix

\[
\begin{bmatrix}
0.9 & 0.1 \\
0.2 & 0.8
\end{bmatrix}
\]

The input binary symbols '0' and '1' occur with probabilities 0.25 and 0.75, respectively. Draw the channel diagram and determine the probabilities of the binary symbols 0 and 1 appearing at the channel output.

3(c). A (5, 2) linear block code has the following code words

\[ C = \{00000, 10100, 01111, 11011\} \]

Determine the generator matrix \( G \), parity check matrix \( H \) and the error correcting capability of the code.

**OR**

3'(a). Let \( X \) and \( Y \) be binary random variables with

\[
P(X = 0, Y = 0) = 1/3, \quad P(X = 1, Y = 0) = 1/3, \quad P(X = 0, Y = 1) = 1/3
\]

Find the mutual information \( I(X; Y) \).

3'(b). In the light of channel capacity theorem, discuss briefly the tradeoffs between channel capacity \( C \), channel bandwidth \( B \) and the SNR.

4(a). Why is there a processing gain in spread spectrum system? How is the processing gain defined for direct sequence spread spectrum?

4(b). Discuss briefly some important attributes of spread-spectrum.

4(c). A direct sequence spread spectrum system is to provide a jamming margin of 20 dB. The required \( E_b/N_0 \) for satisfactory reception for the system is 10 dB. Determine the length of the feedback shift register for the required processing of the system.
2016-17
B.TECH V SEMESTER EXAMINATION
ELECTRONICS ENGINEERING

MICROWAVE AND ANTENNA
(EL – 354)

Max Marks: 60 Credits: 4 Duration: 2 Hours

- Attempt all questions and answer all parts of the questions together.
- Make suitable assumptions if required.
- Symbols and abbreviations have their usual meanings.

1(a) A rectangular waveguide with dimensions 6cm x 4cm operates at 5 MHz in the TM_{11} mode. Compute
   (i) Cutoff frequency \( f_c \)
   (ii) Guided wavelength \( \lambda_g \)
   (iii) Phase velocity \( v_p \)
   (iv) Group velocity \( v_g \)

   For the case when waveguide is filled with a dielectric having \( \mu_r = 1 \) and \( \epsilon_r = 2.1 \).

1(b) What are the lowest possible TE and TM modes in rectangular waveguide and why?

2(a) What is the fundamental difference in the beam-RF interaction in two-cavity klystron amplifier and TWT amplifier?

2(b) A travelling wave tube having a helix characteristic impedance \( Z_0 = 10 \) ohms operates at 10 GHz. Its beam voltage \( V_0 = 5 \text{kV} \), beam current \( I_0 = 40 \text{mA} \) and circuit length \( N = 40 \). Find its
   (i) Gain parameter
   (ii) Output power gain \( A_p \)
   (iii) Phase constant of velocity-modulated electron beam \( \beta_e \)

OR

2(a) Discuss the basic operation principle of travelling wave tubes. Why are slow wave structures required in this tube?

2(b) The magnetron operates at an anode voltage \( (V_0) = 5 \text{kV} \) beam current \( (I_0) \) of 5A and frequency \( (f) \) of 10 GHz. Its resonator conductance \( (G_i) \) is 0.25 milli-mhos, loaded conductance \( (G_l) \) is 0.03 milli-mhos and vane capacitance \( (C) \) is 3 pF. The power loss \( (P_{loss}) \) in the device is 15kW. Calculate
   (i) Angular resonant frequency
   (ii) Unloaded \( Q_{un} \)
   (iii) Loaded \( Q_l \)

Contd...
<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(iv) External $Q_{ex}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(v) Circuit efficiency $\eta_c$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(vi) Electronics efficiency $\eta_e$</td>
<td></td>
</tr>
<tr>
<td>3(a)</td>
<td>Discuss the tunneling phenomena and draw the V-I curve of a tunnel diode under forward bias condition.</td>
<td>07</td>
</tr>
<tr>
<td>3(b)</td>
<td>A parametric amplifier has ratio of its output to input frequency of 30, figure of merit 12, factor of figure of merit 0.5 and diode temperature 300K. Calculate its power gain, noise figure and bandwidth.</td>
<td>08</td>
</tr>
<tr>
<td>OR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3(a*)</td>
<td>Discuss the Ridley-Watkins-Helsum (RWH) theory.</td>
<td>07</td>
</tr>
</tbody>
</table>
| 3(b*) | A parallel strip line has the following parameters: $\varepsilon_{rd}=1.5$, $w=20$ mm, $d=5$ mm. Calculate  
     (i) Characteristic impedance of the strip line  
     (ii) Stripline capacitance  
     (iii) Phase velocity  
     (iv) Phase constant. | 08 |
| 4(a) | Define the terms with the help of diagram.  
     (i) Radiation pattern  
     (ii) Half power beamwidth (HPBW)  
     (iii) Beamwidth between first nulls (BWFN) | 07 |
| 4(b) | What is the maximum power received at a distance of 0.5 km over a free-space 1 GHz circuit consisting of a transmitting antenna with a 25 dB gain and a receiving antenna with 20 dB gain? The transmitting antenna input is 150 W. | 08 |
1(a) For a savings account that pays interest at the rate of 1% per month, if deposits are made on the first of each month at the rate Rs 5000 per month, how much money will there be in the account at the end of one year?

(b) Suppose that the 8-point DFT of a sequence \( x[n] = \{a_0, \ldots, a_7\} \) is given by \( \{A_0, \ldots, A_7\} \). If the 4-point DFT of another sequence \( \{b_0, b_1, b_2, b_3\} \) is \( \{A_0, A_2, A_4, A_6\} \), find \( b_k \)'s in terms of \( a_i \)'s.

OR

(b') Define short term Fourier transform (STFT). Which of the limitations of Fourier transform are eliminated by STFT? Illustrate and prove the following properties of STFT:

(i) Linearity
(ii) Time shifting
(iii) Frequency shifting or modulation

(c) Write a MATLAB program to compute linear convolution of two sequences of length \( N \) using \texttt{fft} and \texttt{ifft} functions.

2 A discrete time high pass filter can be obtained from a continuous time low pass filter by the following transformation \( H(z) = H_d(s) \mid_{s = \frac{1}{1+z^{-1}/(1-z^{-1})}} \).

i Show that the above transformation maps \( j\Omega \)-axis of \( s \)-plane onto the unit circle of the \( z \)-plane.

ii Show that if \( H_d(s) \) is a rational function with all its poles inside the left half \( s \)-plane.
plane, then \( H(z) \) will be a rational function with all its poles lie inside the unit circle of \( z \)-plane.

(iii) Suppose a desired high pass discrete time filter has specifications

\[
|H(e^{i\omega})| \leq 0.01 \quad \text{if} \quad |\omega| \leq \pi/3 \\
0.95 \leq |H(e^{i\omega})| \leq 1.05 \quad \text{if} \quad \pi/2 < |\omega| \leq \pi
\]

Determine the specifications on the continuous time low pass filter so that the desired high pass digital filter results from the above specifications.

OR

2'(a) Find the system function of the system shown in Fig. 1.

![System Diagram](image)

Fig. 1

(b) \( H(z) \) is a rational system function of a stable, causal, LTI system, determine which of the following system functions are representing stable/causal systems.

(i) \( H(z)H^*(z^*) \)  
(ii) \( \frac{d}{dz} H(z) \)  
(iii) \( H(z^{-1}) \).

3(a) What are the merits of FIR filters over IIR filters?

(b) The frequency response of a linear phase FIR filter is given by

\[
H(e^{j\omega}) = e^{-j\omega/2} \cos \frac{\omega}{2} (0.78679 \cos \omega - 0.313320).
\]

Determine the filter coefficients \( \{h[n]\} \).

(c) The frequency response of an ideal band-pass filter is given by

\[
H(e^{j\omega}) = \begin{cases} 
0 & 0 \leq |\omega| < \pi/8 \\
1 & \pi/8 \leq |\omega| < 3\pi/8 \\
01 & 3\pi/8 \leq |\omega| <\pi 
\end{cases}
\]

(i) Show that the impulse response of the filter can be expressed as the product

Contd.....3.
of \cos(n\pi/4) and the impulse response of a low-pass filter.

(ii) Design a length-7 filter using triangular window.

4(a) Explain Booth’s multiplication algorithm for multiplying two fixed point numbers. Multiply 0.75 by 0.625 using Booth algorithm.

OR

(a') Show that the variance of the error in the frequency response, \( \sigma_e^2(\omega) \) of length \( N+1 \) FIR filter due to coefficient quantization (round off to \( b \)-bit magnitude) is bounded as:

\[
\sigma_e^2(\omega) \leq 2^{-2(b+1)} (2N+1)/3
\]

(b) Develop an expression for the output \( y[n] \) as a function of input \( x[n] \) for the multirate system shown in Fig – 2.

\[
\begin{align*}
x[n] & \rightarrow \uparrow 5 \rightarrow \downarrow 10 \rightarrow \uparrow 2 \rightarrow y[n] \\
\text{Fig – 2}
\end{align*}
\]