Q.No. | Question | M.M.
--- | --- | ---
1(a) Using suitable diagrams, describe  
   (i) High state and low state noise margins.  
   (ii) Low to high and high to low propagation delays | [02] | 
1(b) Give three advantages and three disadvantages of ECL | [03] | 
1(c) Using-appropriate values of components, analyse and explain the working of a two input schottkey TTL NAND gate. | [07] | 

OR

1(c') Explain the basic operation of Emitter Coupled Logic (ECL) circuit. Also draw the ECL circuit with addition of an emitter-follower. Why emitter-followers are used in ECL circuits. Also draw ECL OR/NOR gate. | [07] | 

Give the advantages of BiCMOS logic circuit. Sketch and explain the most improved version of BiCMOS inverter. | [08] | 

2(a) Explain the operation of CMOS transmission gate as a switch. Implement a 2-line-to-one-line MUX, using CMOS transmission gate in Pass Transistor Logic. | [6] | 

2(b) What is the concept of “good 1” and “good 0”? | | 

OR

Draw a complete voltage transfer characteristics (VTC) of CMOS inverter, showing all the critical points clearly. How the inverter is designed to have | [6] | 

Contd.....2.
Design a Programmable Logic Device (PLD) for a 4 bit binary to Grey code converter.

3(a) Why a DRAM is refreshed? How does a 3242 DRAM controller performs address multiplexing and refresh address counting for refresh operation in a 16K DRAM?

3(b) Using sense amplifier and equalization circuit, explain READ and WRITE operation of a SRAM cell.

3(c) OR

Explain the signal activity (timing diagram) for WRITE cycle of a DRAM

3'(c) Or

With the help of circuit and timing diagram explain the operation of a Dual-Slope Integrating A/D Converter.

4(a) Using logic circuit and waveforms sketch and explain the circuit of a Digital Voltmeter.

4(b) OR

Sketch the logic circuit of a Digital Storage Oscilloscope (DSO) and explain its operation.
1(a) Design a first order low pass filter such that T(0) = 0.9 and 3-dB frequency is 1MHz. Assume that no power supply is available.

1(b) An impedance function has a pole-zero plot shown in Figure 1. If Z(-2) = -130/16, synthesize the impedance function in:
   i) Cauer's-I form   ii) Cauer's-II form

OR

1(b') A pole-zero pattern of function F(s) is shown in Figure 2. Taking scale factor as 1, synthesize F(s): i) as an impedance in Foster Form   ii) as an admittance in Cauer's Form

1(c) What do you understand by Cascade Realization? What are the merits of cascade approach in filter design?
2(a) Derive the expression for the change in gain due to simultaneous variation in $\omega_z$ and $Q_z$ realizing the second order function:

$$F(s) = s^2 + \frac{\omega_z}{Q_z} s + \omega_z^2$$

What are the factors affecting the gain sensitivity?

2(b) It is required to design a low-pass filter whose requirements are characterized by:

$$A_{max} = 0.5 \text{ dB} \ ; \ A_{min} = 12 \text{ dB} \ ; \ \omega_p = 100 \text{ rad/s} \ ; \ \omega_s = 400 \text{ rad/s}$$

Find out the order of Butterworth filter.

2(c) Show that the Chebyshev Approximation provides more stop-band attenuation than Butterworth approximation for the same order of function.

OR

2(c') For a maximally flat second-order low-pass filter ($Q = \frac{1}{\sqrt{2}}$); show that at $\omega = \omega_o$, the magnitude response is 3-dB below the value at dc.

3(a) Sketch the circuit for positive feedback topology and derive the expression for its transfer function.

3(b) Give the circuit of Antoniou general impedance converter (GIC). Show that how GIC can realize a grounded frequency dependent negative resistance (FDNR).

3(c) Synthesize the second order low pass filter to have a pole frequency of 2 KHz and a pole $Q$ of 10 using Saraga design of the Sallen and Key circuit. Also compute the component sensitivities with respect to $\omega_o$ and $Q$.

OR

3(c') Design a Kerwin-Huelsman-Newcomb (KHN) circuit to realize a high pass function with $f_0 = 10$ KHz and pole $Q = 10$. Choose $C=1nF$. What is the value of high frequency gain obtained. Also draw the resulting circuit.
4(a) What are the merits of \( g_m \)-C filters over operational amplifier based RC circuits.

4(b) Analyze the voltage-mode circuit given in Figure 3 to obtain the expression of universal bi-quadratic filter and find out the various filter functions realized.

![Figure 3](image)

4(b') Analyze the current-mode bi-quadratic filter shown in Figure 4.

i) Identify the filter function realized.

ii) Give the expression of filter parameters.

![Figure 4](image)

4(c) What are tuned amplifiers? Describe the function of a single-tuned amplifier with the help of a circuit diagram.

OR

4(c') What is a mixer? Draw and analyze the circuit of an op-amp based mixer. Also, mention the applications of mixer circuits.
Answer all the questions.
Assume suitable data if missing.
Notations and symbols used have their usual meaning.

Q.No.          Question

1(a) With a suitable example, explain the difference between Uniprocessor, Pipelined, and Parallel Architectures. [06]

1(b) Implement the Boolean expression given below, with only NAND gates, and identify the critical path in the obtained circuit.

\[ F = \overline{A} \overline{B} + C \overline{D} (\overline{A} + B) + BC \] [09]

2(a) What is meant by Logical effort of a gate? Compute the logical effort associated with circuits shown in Figure – 1 and in Figure – 2. Assume all PMOS transistors have aspect ratios three times that of NMOS transistors. [05]

2(b) Draw a colored layout for any one of the circuits shown in Figure 3. Use the design rules for a Double – Metal, Double – Polysilicon, n – well, bulk CMOS process. [10]

3 Write short technical notes on any FOUR of the following: [15]
1. Mask Making and Printing Defects
2. Yield of IC Processes
3. Photolithography
4. Wet and Dry Etching
5. Wet and Dry Oxidation
6. Doping by Diffusion
7. Ion Implantation
8. Metallization

Contd....2.
4(a) With suitable diagrams, explain the following isolation techniques:

i. Guard Ring

ii. Shallow and Deep Trench

4(b) What are the advantages offered by the following alternatives to the CMOS technology:

a. Silicon-on-Insulator (SOI)

b. Gallium Arsenide (GaAs)

Figure 1

Figure 2

Figure 3: Draw the layout for any ONE of the above circuits
Q.No.  Question                                      M.M.
1(a) Draw the block diagram of a microprocessor based computer system showing
      the address, data and control bus structure. [08]

   OR

1(a)* Describe the internal registers in 8085 microprocessor including their abbreviations,
      size, and their primary functions. [08]

1(b) Specify the content of the accumulator and carry flag when the following
      instructions are executed.
      MVI A, C5H
      ORA A
      RAL
      RRC
      [07]

2(a) Mention various types of interrupts in 8085. Give their respective priorities,
      trigger mode (edge or level) and interrupt type (vectored or non-vectored). [07]

2(b) What is handshaking? Why and how it is done? What are its advantages? [08]

   OR

2(b)* What is the function of 8259? How many initialization command words are used
      in it? Explain them. [08]

3(a) Draw a memory address decoder circuit using 74LS138 for a 2K RAM starting
      from B000 H. [07]
3(b) Write Instructions to define port A as input port in Mode 0, Port B as output port in Mode 1 and Port C_upper as input, 8255 address starts from 60H.

OR

3(b)' Draw & explain functional pin diagram of 8251 USART.

4(a) Write short notes on any two.

   i) MDS
   ii) Simulator
   iii) Logic Analyzer

4(b) Describe the generation of 20 bit memory address in 8086 microprocessor.
2015-16
B.TECH. (AUTUMN SEMESTER) EXAMINATION
ELECTRONICS ENGINEERING
MICROPROCESSORS & MICROCOMPUTERS
EL-332

Maximum Marks: 60
Credits: 04
Duration: Three Hours

Answer all the questions.
Assume suitable data if missing. Question No 1 to 3 are related to 8085A and its related peripherals.
Notations and symbols used have their usual meaning.

Q.No. | Question
--- | ---
1(a) | i) The addressing of Instruction “LDA X B” is
   | A) Immediate
   | C) Register Indirect
   | B) Register Direct
   | D) Direct
   
   ii) If A > B the execution of the instruction “CMP B” will result in values of Cy and Z flagsds :
   | A) Cy=1, Z=1
   | C) Cy=1, Z=0
   | B) Cy=0, Z=0
   | D) Cy=0, Z=1
   
   iii) The maximum number of T-states in op-code fetch machine cycle could be
   | A) 3 T-states
   | C) 5 T-states
   | B) 4 T-states
   | D) 6 T-states

1(b) Note: Answers should be brief and to the point
   i) What will be the contents of Accumulator and status flag Cy when the program given below is executed:
      2000 MVI A, 80H
      2002 MVI B, 89H
      2004 ADD B
      2005 RRC
      2006 HLT
      
      [1.5]
   
   ii) What do you understand by “WAIT State”? Draw a labelled timing diagram for Op-Code fetch machine cycle with one WAIT state.
      [2.5]
   
   iii) Write an 8085 program to transfer a block of data stored in memory location 2500H-2509H to the memory location 3500H onwards.
      [2.5]
1(c) The following algorithm converts an n-bit binary number $b_{n-1}, b_{n-2}, \ldots, b_0$ to n-bit gray code.

$\overline{g_{n-1}}, \overline{g_{n-2}}, \ldots, \overline{g_0}$ such that $g_{n-1} = b_{n-1}$ for most significant bit and $g_i = b_{i+1} \oplus b_i$ for $0 < i < n-1$.

Write a program that inputs an 8-bit binary number and converts it into its equivalent gray code using the above algorithm.

OR

1'(c) Draw the Architectural block diagram of 8085A microprocessor and explain the function of Trap, RST7.5, RST6.5 and RST5.5 pins in it.

2(a) i) The programmed data transfer is used mainly when:

A) Small amount of data is transferred using relatively slow I/O devices.
B) Small amount of data is transferred using relatively fast I/O devices.
C) Large amount of data is transferred using relatively slow I/O devices.
D) None of this is true

ii) Bit 15 and Bit 14 in the count register of 8257 DMA controller are at logic '1'. It signifies

A) Verify Transfer
B) Write Transfer
C) Read Transfer
D) Illegal operation

iii) 8259A Programmable interrupt controller is

A) 40 PIN IC  B) 28 PIN IC  C) 24 PIN IC  D) 20 PIN IC

2(b) Note: Answers should be brief and to the point

i) Give the format of RIM Instruction and explain the function of each bit present in it.

ii) How many types of polling is there? Explain the software polling using the Device polling algorithm and the circuit for software polling.

iii) 8259A PIC is connected to 8085A microprocessor. What will be the sequence of events that will occur when one or more interrupt requests goes high requesting the service?

2(c) What is the need for DMA transfer? With the help of a flow chart explain the operation of DMA controller for transferring the Data from I/O device to Memory using cycle stealing mode.

OR

2'(c) Differentiate between Initialization command word and Operational command word. In a programmable Interrupt controller the initialization command words (ICW) and operational command words (OCW) are;

$ICW1 = (00001001)_b, \quad ICW2 = (11111111)_b \quad \text{and} \quad OCW1 = (10001010)_b$

Contd.....3.
i) How many PIC's are cascaded?

ii) What is the CALL Address Interval between Interrupts?

iii) Whether the interrupts are Edge triggered or Level triggered?

iv) What addresses are assigned to IRo to IR3 Interrupts?

v) Which Interrupts are masked?

3(a)

i) The number 98H written in the control word register of 8255 PPI means;

A) Port A, Port C_up, Port B and Port C_low are input ports

B) Port A, Port C_up are input and Port B, Port C_low are Output ports

C) Port A, Port C_up are output and Port B, Port C_low are input ports

D) Port A, Port C_up are output and Port B, Port C_low are output ports

ii) For 8251 USART in mode word for Asynchronous mode, the bits L2,L1=(10)B means;

A) Five bits/Character

B) Six bits/Character

C) Seven bits/Character

D) Eight bits/Character

iii) Control word register of 8253 timer/counter is of

A) 8 bits

B) 6 bits

C) 16 bits

D) None of these

3(b)

Note: Answers should be brief and to the point

i) Give the control word format of 8253 Programmable interval timer and give the significance of each bit in it.

ii) What is the need for interfacing? Discuss in brief various incompatibilities that may prevent the microprocessor to transfer data to/from memory and I/O devices.

iii) Differentiate between Synchronous and Asynchronous serial data transmission.

3(c)

Explain different configurations of 8255A in Mode 1.

OR

3*(c)

A microprocessor is to be interfaced with Memory and I/O devices in memory mapped I/O mode. A total of 8K EPROM starting from Memory location 0000H and 48K RAM starting from memory location 2000H onwards is to be interfaced. In addition two I/O devices also have to be connected. Assume that both RAM and EPROM are available in the blocks of 8K each. Design a decoding circuitry using a 3X8 decoder and show its implementation.

4(a)

i) The addressing capability of 8086 microprocessor is;

A) 64KB

B) 1 MB

C) 16 MB

D) 64 MB

ii) On chip ROM and RAM in 8051 microcontroller is respectively;

A) 1KB and 128 Byte

B) 1KB and 256 Byte

C) 4KB and 128 Byte

D) 4KB and 256 Byte

Contd.....4.
iii) The number of input output lines available in 8051 microcontroller are:

A) 16 Lines  B) 24 Lines  C) 28 Lines  D) 32 Lines

4(b) Note: Answers should be brief and to the point

i) Give the format of flag register of 8086 Microprocessor with suitable explanation of additional flags.

ii) Give a brief account of comparison between 8951 family of microcontrollers.

iii) Give the format of TMOD and TCON registers. What will be the timer/counter configuration if TMOD register have a value 03H.

4(c) Draw the internal block diagram of 8051 microcontroller. Explain the function of each pin of it.

OR

4'(e) Using the timer 1 in mode 1; Assuming TH1=00H and TL1=FFH

1) Write a program to generate a square wave of 50% duty cycle on P1.5 pin.

2) Find the frequency of generated waveform

Assume that the crystal frequency is 11.0592MHz.
2015 – 2016
B Tech (Autumn Semester) Examination
(Electronics Engineering)
Principles of Communication Engineering
EL – 341
Credits: 4

Maximum Marks: 60

Duration: Three Hours

Notes:
1. Answer all questions.
2. Any missing information can suitably be assumed.

1. (a) Determine the pre-envelope \( g_s(t) \) of the signal \( g(t) = [1 + k \cos(2\pi f_m t)] \cos(2\pi f_c t) \).
(b) Write down the expressions of the transfer functions of the linear filter channels having
   (i) zero phase
   (ii) linear phase.
(c) Draw the block diagram of a super heterodyne radio receiver.
(d) An angle modulated signal is described by, \( s(t) = 100 \cos[2\pi 10^7 t + 4 \sin 2000\pi t] \).
   (i) Determine the average transmitted power.
   (ii) Determine the peak phase and frequency deviations.
   (iii) Is this an FM or a PM signal? Explain.

OR

1' (a) How should you select the charging and discharging time constants of an envelope detector for its satisfactory operation?
(b) Why do you need more than one stage of modulation in SSBSC schemes?
(c) Explain, with the help of a block diagram and suitable analysis, the working of a PLL as an FM demodulator.

2. (a) State Nyquist sampling theorem.
(b) The signal \( g(t) = \cos \omega_0 t + \cos 8 \omega_0 t \) is sampled using natural sampling. What is the minimum sampling rate \( f_s \)? Sketch the sampled signal \( s(t) = g(t)x(t) \), if \( x(t) \) is the train of pulses having unit height, occurring at the rate \( f_s \); and \( x(t) = 1 \) for \( nT_c - \pi/2 \leq t \leq nT_c + \pi/2 \). Given that the pulse duration \( T \) is
   (i) \( 1/32f_0 \).
   (ii) \( 1/320f_0 \).
(b') A signal \( x(t) \) undergoes a zero-order hold operation with an effective sampling period \( T \) to produce a signal \( x_0(t) \). Let \( x_1(t) \) denotes the result of a first-order hold operation on the samples of \( x(t) \); i.e.,

\[
x_1(t) = \sum_{n=-\infty}^{\infty} x(nT) h_1(t - nT),
\]

where \( h_1(t) \) is shown in Fig - 1. Specify the frequency response of a filter that produces \( x_1(t) \) as its output when \( x_0(t) \) is the input.

(c) Explain why quantization noise could affect small amplitude signals in a PCM system far more than large signals. Suggest some method of improvement in this regard.

3 (a) List three properties of narrow-band noise and provide their proses.
(b) Prove that the additive noise appearing at the FM discriminator output is determined effectively by the carrier amplitude and the quadrature component of the narrow-band noise.

OR

(b') Explain the terms:
(i) Figure of Merit of a modulation scheme
(ii) FM threshold effect
(iii) Preamphasis and deemphasis

4 (a) Sketch the waveforms for the sequences 1010001111 using following formats:
(i) Unipolar NRZ (ii) Polar NRZ (iii) AMI (iv) Manchester coding
(b) Determine the output of the matched filter of the pulse \( p(t) \) when the input waveform is \( s(t) = A[p(t) - p(t - T_b)] \), where \( p(t) \) is the square pulse of unit amplitude and duration \( T_b \).
(c) What is the significance of an eye pattern? How do you obtain an eye pattern on the CRO screen? Draw a typical eye pattern for binary polar signal and explain how the following parameters can be determined from this diagram: distortion, noise margin, best sampling time, rise time, sensitivity to timing error, time jitter.
1(a) Determine the signal space representation of the four signals shown in Figure 1. Plot the signal space diagram and show that this signal set is equivalent to that of a 4-PSK signal.

![Signal space diagram]

Fig. 1

1(b) In a binary digital communication system, bits ‘1’ and ‘0’ are transmitted using waveforms of amplitude +0.5 V and -0.5 V, respectively over an AWGN channel with zero mean and variance $0.1 \text{ V}^2$. Determine the optimum detection threshold, if the a priori probability of bit ‘0’ is 0.8.

1(c) Consider the detector shown in Figure 2. The channel noise $w(t)$ is white with power spectral density (PSD) of $N_0/2 = 10^{-20} \text{ W/Hz}$. The low-pass filter is ideal with unity gain and cut-off frequency 1 MHz. The input to the decision device is

$y = w$ if transmitted bit is ‘0’

$y = a + w$ if transmitted bit is ‘1’

where $w$ represents the noise sample value. The noise sample has a probability

Contd.....2.
density function, \( p(w) = 0.5 \alpha e^{-\alpha |w|} \) with zero mean and variance \( 2/\alpha^2 \). Assume transmitted bits to be equiprobable and threshold \( \lambda \) is set to \( 10^{-6} \) V. Determine the value of parameter \( \alpha \) and also, the average probability of bit error.

![Diagram](image)

**Fig. 2**

2(a) Consider a 4-PSK constellation with \( d_{\text{min}} = \sqrt{2} \). Calculate the additional energy required to send one extra bit (8-PSK) while keeping the same minimum distance (and thus with the same bit error probability).

2(b) Consider a channel that adds white Gaussian noise of spectral density of \( N_0/2 = 10^{-8} \) W/Hz to a digitally modulated signal. A bit error probability of \( 10^{-5} \) is desired and the data rate is 100 kbps. Find the required average power for the received carrier for coherent binary ASK and FSK modulations.

2(c) The signal component of a coherent PSK system is defined by

\[
s(t) = A_c k \sin(2\pi f_c t) \pm A_c \sqrt{1-k^2} \cos(2\pi f_c t) \quad 0 \leq t \leq T_b
\]

where the plus sign corresponds to symbol '1' and the minus sign to symbol '0'. The first term represents a carrier component included for the purpose of synchronizing the receiver to the transmitter. Suppose that 20 percent of the transmitted signal power is allocated to the carrier component. Determine the average probability of bit error in the presence of AWGN of zero mean and PSD of \( N_0/2 \).

**OR**

2(e) In a coherent FSK system, the signals \( s_1(t) \) and \( s_2(t) \) representing symbols '1' and '0', respectively, are defined by

\[
s_1(t), s_2(t) = A_c \cos \left[ 2\pi \left( f_c \pm \frac{f_c}{2} \right) t \right] \quad 0 \leq t \leq T_b
\]

---

Contd.,...3.
Assuming that $f_c > \Delta f$, show that the correlation coefficient of the signals $s_1(t)$ and $s_2(t)$ is approximately given by

$$\frac{\int_0^{T_h} s_1(t)s_2(t)dt}{\int_0^{T_h} s_1^2(t)dt} \approx \sin c(2\Delta f T_h)$$

Also, determine the minimum value of frequency shift $\Delta f$ for which the two signals are orthogonal.

3(a) A source has infinitely large set of outputs with probability of occurrence $2^i$, $i = 1, 2, 3, \ldots$. Compute the entropy of the source.

3(b) The channel matrix of a BSC channel is given by

$$\begin{bmatrix} 1-p & p \\ p & 1-p \end{bmatrix}$$

The a priori probability of one of the symbol is $\alpha$. Determine the average mutual information $I(X; Y)$ of the channel. Also, determine the value of $I(X, Y)$ for $\alpha = 0.4$ and $p = 0.2$.

3(c) An analog signal having 4 kHz bandwidth is sampled at 1.25 times the Nyquist rate, and each sample is quantized into one of 256 equally likely levels. Assume that the successive samples are statistically independent. Find the bandwidth required for an AWGN channel for error-free transmission of this data if the SNR is 20 dB.

**OR**

3'(a) A binary erasure channel is described by the channel matrix

$$\begin{bmatrix} 1-p & p & 0 \\ 0 & p & 1-p \end{bmatrix}$$

Draw the channel diagram and determine the capacity of the channel.

3'(b) In a single-parity-check code, a single parity bit is appended to a block of $k$ data bits. The single parity bit is chosen so that the code word satisfies the even parity rule. For $k = 3$, set up all possible code words and determine the error pattern(s) that can be detected by the code.

3'(c) An analog signal having 15 kHz bandwidth is sampled at 40 kHz, and each sample

---

Contd...
is quantized into one of 256 equally likely levels. Assume that the successive samples are statistically independent. Find the SNR required for an AWGN channel with a bandwidth of 40 kHz for error-free transmission of this data.

4(a) Why is there a processing gain in spread-spectrum system? How is the processing gain defined?

4(b) Determine the statistics of the direct-sequence spread spectrum receiver noise after it is multiplied by the spreading sequence.

4(c) The information rate of a direct-sequence spread spectrum system is 10 kbps. The chip rate is 10 Mbps. The QPSK-based system is required to have a probability of error due to externally generated interfering signals that does not exceed $10^{-6}$. Calculate the jamming margin in decibels.

4(d) Input data at 150 kbps is modulated using 8-ary FSK. The FSK symbols are then spread by frequency hopping at a rate of 2000 hops/s. Calculate the chip rate.
2015-16  
B.TECH. (AUTUMN SEMESTER) EXAMINATION  
ELECTRONICS ENGINEERING  
MICROWAVE & ANTENNA  
EL-354

Maximum Marks: 60  
Credits: 04  
Duration: Three Hours

Answer all the questions.  
Assume suitable data if missing.  
Notations used have their usual meaning.

<table>
<thead>
<tr>
<th>Q.No.</th>
<th>Question</th>
<th>M.M.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1(a)</td>
<td>Why scattering (S) parameters are used for characterization of microwave devices? Calculate $S_{22}$ and $S_{21}$ for the series element (Z) shown in Fig. 1.</td>
<td>[05]</td>
</tr>
<tr>
<td><img src="image" alt="Fig. 1" /></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1(b)</td>
<td>With the help of appropriate circuit diagram, briefly explain the measurements of VSWR at microwave frequency.</td>
<td>[05]</td>
</tr>
<tr>
<td>1(c)</td>
<td>Briefly explain the directivity and isolation used to characterize a directional coupler. What will be their value for an ideal directional coupler?</td>
<td>[05]</td>
</tr>
<tr>
<td>2(a)</td>
<td>Explain how oscillations are sustained in the cavity magnetron, with suitable sketches, assuming that the π-mode oscillations already exists. Make it clear why more energy is given to the RF field than taken from it.</td>
<td>[05]</td>
</tr>
</tbody>
</table>
| 2(b) | Derive an expression for electron transit time in drift space for two-cavity klystron. Why do practical klystron amplifiers generally have more than two cavities? A two-cavity amplifier klystron has the following parameters:  
Beam current: $I_0 = 30$ mA  
Beam voltage: $V_0 = 900$ V  
Frequency: $f = 8$ GHz | [10] |
<table>
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<tr>
<th>Question</th>
<th>Text</th>
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<tbody>
<tr>
<td>2(a)</td>
<td>Briefly compare the applications of the multi-cavity klystron, reflex klystron and magnetron. Mention two most significant advantages of each tube.</td>
</tr>
</tbody>
</table>
| 2(b) | i) Show that circuit efficiency ($\eta_c$) in a Magnetron oscillator is given by \[ \eta_c = \frac{1}{1 + Q_{ext}/Q_{unloaded}} \] Where $Q_{ext}$ is the external quality factor and $Q_{unloaded}$ is the unloaded quality factor.  

ii) Draw an Applegate diagram of a reflex klystron operating in $2\frac{3}{4}$ mode. 

iii) What do you mean by optimum length ($L_{opt}$)? Derive expression for $L_{opt}$ for klystron amplifier having two-cavities. |
<p>| 3(a) | Why tunnel diode has improved noise performance? The equivalent circuit of tunnel diode negative resistance amplifier is shown in Fig. 2. With appropriate circuit analysis show that amplification will occur when $g &lt; 4g_L$. |
| 3(b) | What is two valley theory? If $\mu_L$ and $\mu_U$ are the mobilities of electron in lower and upper valley, respectively, then explain why $\mu_L$ is higher than $\mu_U$? |
| 3(c) | Can varactor mechanism be achieved by changing inductance or any other circuit parameter? What are the relative advantages of these techniques? |</p>
<table>
<thead>
<tr>
<th>Question</th>
<th>Answer</th>
</tr>
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</table>
| 3'(a) | Using Manley-Rowe power relation to show that for up-converter parametric amplifier power gain, \( G \) can be expressed as:  
\[
G = \left( \frac{f_p + f_s}{f_s} \right) 
\]  
where \( f_p \) = pump signal frequency and \( f_s \) = signal source frequency |
| 3'(b) | What are the different types of Strip-line? Enumerate the advantages and disadvantages of such line with respect to waveguides and coaxial lines. |
| 3'(c) | What is the major drawback of avalanche devices? What limitation does this place on their applications? |
| 4(a) | What makes an Antenna? Show that E-field due to Hertzian antenna in vicinity at a distance \( r \) from the antenna is proportional to inverse of \( r^3 \) and \( r^2 \) |
| 4(b) | What do you mean by radiation resistance? Determines its value for dipole antenna having length equal to \( \lambda \). |
| 4(c) | Write short notes on the following:  
i) Broad side array  
ii) End Fire array |