2016-17  
B.TECH. (AUTUMN SEMESTER) EXAMINATION  
COMPUTER ENGINEERING  
OBJECT ORIENTED PROGRAMMING  
CO-203

Maximum Marks: 60  
Credits: 04  
Duration: Two Hours

Answer all the questions.  
Assume suitable data if missing.  
Notations used have their usual meaning.

Q.No.  
Question  
M.M.

1  
Attempt any two of the following:  

1(a) Discuss about the key concepts of object oriented programming.  
[7.5]  
1(b) Explain the concept of constructor and destructor with example programs in C++.  
[7.5]  
1(c) What is meant by overloading and overriding of function? Explain it with an example program.  
[7.5]

2  
Attempt any two of the following:  

2(a) What is virtual function? Give rules for virtual functions.  
[7.5]  
2(b) What is generic programming? How is it implemented in C++?  
[7.5]  
2(c) What are the different forms of inheritance? Give an example for each  
[7.5]

3  
Attempt all parts  

3(a) Write a program in java to implement bubble sort. Consider the following points in the program:  
[7.5]  
   i. Initialization using constructor  
   ii. Implement operations using methods  
3(b) Define applets in java and discuss its life cycle. Write an example applet program, how you could invoke an applet.  
[7.5]

4  
Attempt 4 or 4'  

4(a) Draw one-shot state diagram for chess game.  
[7.5]  
4(b) Prepare a class diagram from the given object diagram:  
[7.5]  
cont'd... 2.
4'(a) Prepare a class model to describe undirected graphs. An undirected graph consists of a set of vertices and a set of edges. Edges connect pairs of vertices. Your model should capture only the structure of graph (i.e. connectivity), and need not be concerned with geometrical details such as location of vertices or lengths of edges. A typical graph is shown in figure below.

4'(b) Discuss scenario and sequence diagram with example.
2016-17
B.TECH. (AUTUMN SEMESTER) EXAMINATION
COMPUTER ENGINEERING
ALGORITHMS AND DATA STRUCTURE
CO-206

Maximum Marks: 60
Credits: 04
Duration: Two Hours

Answer all the questions.
Assume suitable data if missing.
Notations used have their usual meaning.

Q.No. Question M.M.

1(a) With the help of a suitable example, explain the steps involved in designing a recursive algorithm. [07]

1(b) Prove that for every polynomial $P(n) = a_0 + a_1n + a_2n^2 + \ldots + a_mn^m$ of degree $m$, where $a_m > 0$, $P(n) = O(n^m)$. [08]

OR

1'(a) Suppose a function $f_1(n)$ is $O(g_1(n))$ and $f_2(n)$ is $O(g_2(n))$. Prove that, $f_1(n) + f_2(n)$ is $O(\max(g_1(n),g_2(n)))$. [07]

1'(b) What is Tower of Hanoi Problem? How is it solved recursively? Write the recurrence relation and determine the time complexity of the recursive solution. [08]

2(a) Given a pointer ‘p’ to the starting node of a linear linked list, write an algorithm to delete the last element from the list. [07]

2(b) Convert the following infix expression to postfix showing all the steps involved:

$$A+(((B-C)*(D-E)+F)/G)\$(H-J))$$.

OR

2'(a) Evaluate the following postfix expression: $6\ 2\ 3\ -\ 3\ 8\ 2\ /\ +\ 2\ \$$\ 3\ +$

Show the steps involved. [07]

2'(b) Show how a stack can be implemented using a linear linked list. Write algorithms. [08]
for Push and Pop operations.

3(a) Sort the following sequence of numbers in ascending order using selection sort. [07]
Show the passes involved.

77, 33, 44, 11, 88, 22, 66, 55

Is selection sort a stable sorting algorithm? Justify your answer.

3(b) Show how Binary search can be applied to search the integer 11 in the following [08]
array $A[0...10]$ of integers.

$$
\begin{array}{ccccccccccc}
7 & 11 & 13 & 18 & 21 & 27 & 35 & 39 & 48 & 57 & 65 \\
\end{array}
$$

What is the best case, worst case and average case time complexity of Binary Search for an input of size ‘n’. What are the limitations of Binary Search?

4(a) Explain the following terms giving one example of each: [07]

i. Completely connected graph.

ii. Strongly connected graph.

4(b) Construct a binary search tree from the elements in the order given below: [08]

14, 15, 4, 9, 7, 18, 3, 5, 16, 20, 17, 21, 13, 11, 25

For the tree so obtained write the inorder, preorder and postorder traversal.

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**2016-17**  
**B.TECH. (AUTUMN SEMESTER) EXAMINATION**  
**COMPUTER ENGINEERING**  
**LOGIC THEORY & COMPUTER ORGANIZATION**  
**CO-207**  

**Maximum Marks: 60**  
**Credits: 04**  
**Duration: Two Hours**

*Attempt all the questions. Assume suitable data if missing. Notations used have their usual meaning.*

<table>
<thead>
<tr>
<th>Q.No.</th>
<th>Questions</th>
<th>M.M.</th>
</tr>
</thead>
</table>
| 1(a) | Using Boolean Algebra (postulates and theorems), simplify the following functions to a minimum number of literals.  
(i) $A + A' B$  
(ii) $AB + A'C + BC$  
(iii) $(A + B) (A' + C) (B + C)$ | [05] |
| 1(b) | Express the Boolean function, $F = xy' + x'z$ in a product of maxterm form. | [05] |
| 1(c) | Show that the dual of exclusive-OR is equal to its complement. | [05] |
| 2(a) | Using Karnaugh map simplify the following Boolean function $F$ together with the don't-care conditions $d$.  
$F(A,B,C,D) = \Sigma (4, 5, 7, 12, 13, 14)$  
$d(A,B,C,D) = \Sigma (1,9,11,15)$ | [05] |
| 2(b) | Write down/derive the expressions for the Sum and Carry terms of 4-bit full adder with look-ahead carry.  
Using the expressions for Carry term derived above, show (compute) the value of final carry generated for the above 4-bit full adder when two numbers added are :  
A: 1111 and B: 0001 (Assuming initial carry $C_i = 1$). | [10] |
| 2(b') | Construct a 4-bit BCD adder using two 4-bit binary adders and external gates. Draw the necessary circuit diagram. | [10] |
| 3(a) | What do you mean by triggering of flip-flop? Draw Logic diagram of a clocked master-slave flip-flop. Explain its operation. | [05] |
### 3(b)
Using JK flip-flops design a 3-bit counter that has a repeated sequence of following six states. Also draw the state diagram and circuit/logic diagram of the counter.

000, 001, 010, 100, 101, 110

### 3(b')
Design a sequential circuit with JK flip-flops to satisfy the following state equation:

\[
\begin{align*}
A(t+1) &= A' B' CD + A' B' C + ACD + A C' D' \\
B(t+1) &= A' C + C D' + A' B C' \\
C(t+1) &= B \\
D(t+1) &= D'
\end{align*}
\]

### 4(a)
What do you mean by macro-operations and micro-operations in a digital system? List and explain various categories of micro-operations most often encountered in a digital system.

### 4(b)
A simple computer is capable to execute the following instructions

(i) **MOV R**  (Move R to A)
(ii) **LRI OPRD** (Load OPRD into R)
(iii) **LDA ADRS** (Load Operand specified by ADRS into A)

Draw the block diagram of the simple computer and write the **micro-operations** for Instruction Fetch Cycle, and Execution of the above three instructions.

### 4(b')
Using block diagram and timing diagram, describe and explain the circuits to Generate

(i) Word-time signals, and
(ii) Timing Signals using a ring counter
Question 1.

i. Sketch the cross-sectional view of an n-channel and p-channel enhancement type MOSFET.

ii. With the knowledge that $\mu_n = 2.5 \mu_p$, what must be the relative width of $n$-channel and $p$-channel devices if they are to have equal drain currents when operated in the saturation mode with overdrive voltage of the same magnitude? Assuming equal channel lengths of the devices and neglect channel length modulation.

OR

i'. The terminal voltages of various $nnp$ transistors are measured during operation in their respective circuits with the results given in Table 1, where the entries are in volts, 0 indicates the reference terminal to which the black (negative) probe of the voltmeter is connected. For each case, identify the mode of operation of the transistor.

<table>
<thead>
<tr>
<th>Case</th>
<th>E</th>
<th>B</th>
<th>C</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0.7</td>
<td>0.7</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0.8</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>-0.7</td>
<td>0</td>
<td>0.7</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>-0.7</td>
<td>0</td>
<td>-0.6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>-2.7</td>
<td>-2.0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>5.0</td>
<td></td>
</tr>
</tbody>
</table>

Table 1

Question 2.

i. Draw the small-signal circuit models for the n-channel MOSFET
   a) Neglecting the effect of the channel length modulation.
   b) Including the effect of the channel length modulation.

ii. The transistor amplifier shown in figure 1 is biased with a current source $I$ and has a very high $\beta$. Find the value of $g_m$. Replace the transistor with the simplified hybrid-$\pi$ model for small signal operating and hence find the voltage gain $v_c/v_i$.

![Figure 1](image-url)
Question 3.

i. For an n-channel MOSFET with \( t_{ox} = 10 \text{ nm} \), \( L = 1.0 \text{ \mu m} \), \( W = 10 \text{ \mu m} \), \( L_{ov} = 0.05 \text{ \mu m} \), \( C_{sb0} = C_{db0} = 10 \times 10^{-15} \text{ F} \), junction built-in voltage \( V_0 = 0.6 \text{ V} \), \( V_{SB} = 1 \text{ V} \), and \( V_{DS} = 2 \text{ V} \), calculate the following capacitances when the transistor is operating in saturation: \( C_{ox}, C_{ov}, C_{gs}, C_{gd}, C_{sb}, \) and \( C_{ab} \). (Assume \( \varepsilon_{ox} = 3.45 \times 10^{-11} \text{ F/m} \)).

ii. Derive the expression for the unity-gain frequency \( f_T \), for the high-frequency operation of the MOSFET as an amplifier. (The unity-gain frequency is defined as the frequency at which the short-circuit current gain of the common-source configuration becomes unity)

\[ \text{Figure 2} \]

OR

ii. Find the midband gain \( A_M \) and the upper 3-dB frequency \( f_H \) of a CS amplifier (Figure 2) fed with a signal source having an internal resistance \( R_{sig} = 100 \text{ k\Omega} \). The amplifier has \( R_C = 4.7 \text{ M\Omega} \), \( R_D = R_L = 15 \text{ k\Omega} \), \( g_m = 1 \text{ mA/V} \), \( r_o = 150 \text{ k\Omega} \), \( C_{gs} = 1 \text{ pF} \), and \( C_{gd} = 0.4 \text{ pF} \).

Question 4.

i. List three advantages of negative feedback in an amplifier design.

OR

i. A Colpitts oscillator is designed with \( C_1 = 100 \text{ pF} \) and \( C_2 = 7500 \text{ pF} \). Determine the range of inductor for the frequency to vary from 950 to 2050 kHz.

ii. (a) An electronic system has a gain of 80 dB without feedback. If the negative feedback fraction is 1/50th. Calculate the closed-loop gain of the system in dB with the addition of negative feedback.

(b) If after 5 years the loop gain of the electronic system without negative feedback has fallen to 60dB and the feedback fraction has remained constant at 1/50th. Calculate the new closed-loop gain value of the system.

OR

ii. In a Hartley’s oscillator, the inductor \( L_1 \) and \( L_2 \) have a mutual inductance \( M \). Show that the frequency of oscillation is given by

\[ \Omega_o = \left[ C(L_1 + L_2 + 2M) \right]^{-\frac{1}{2}} \]

\[ \text{Contd... 3.} \]
Question 5. [6 x 2=12 Marks]

i. For the fixed bias circuit as shown in figure 3. Where, \( R_C = 2.2 \, k\Omega \), \( I_B = 40 \, \mu A \), \( I_E = 4 \, mA \), and \( V_{CE} = 7.2 \, V \). Determine: (a) \( I_C \), (b) \( V_{CC} \), (c) \( \beta \), (d) \( R_B \).

ii. In the circuit of figure 4, let \( R_G = 10 \, M\Omega \), \( R_D = 10 \, k\Omega \), and \( V_{DD} = 10 \, V \). For each of the following two transistor find the voltages \( V_D \) and \( V_G \).

a) \( V_t = 1 \, V \) and \( k_n(W/L) = 0.5 \, mA/V^2 \),

b) \( V_t = 2 \, V \) and \( k_n(W/L) = 1.25 \, mA/V^2 \).

OR

ii'. For the self-bias circuit shown in figure 5, show that

\[
\frac{dI_C}{dV_{BE}} = \frac{-\beta/R_E}{R_B/R_E + (1 + \beta)}
\] where, \( R_B = R_1//R_2 \)

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End of Question Paper
2015-2016
B.TECH AUTUMN (III SEMESTER) EXAMINATION
(COMPUTER ENGINEERING)
EL-211
ELECTRONIC DEVICES AND CIRCUITS
CREDITS: 04

Maximum Marks: 60
Duration: Three Hours

1. Attempt all questions
2. Make appropriate assumptions if required
3. Symbols and abbreviations have their usual meanings.

Q1. (a) Explain the construction and working of the tunnel diode. How is the negative resistance region used in the design of oscillator? (6)

(b) The NMOS and PMOS transistors in the circuit shown in Fig. 1 are matched with
\[ K_n \left( \frac{W_n}{L_n} \right) = K_p \left( \frac{W_p}{L_p} \right) = 1mA/V^2 \quad \text{and} \quad V_{T_n} = -V_{T_p} = 1V. \]
Assuming \( \lambda = 0 \) for both devices, find the drain currents \( i_{DN} \) and \( i_{DP} \) and the voltage \( v_o \) for \( v_I = -2.5V \).

Q2. (a) Assume that a silicon transistor with \( \beta = 50 \), \( V_{BE} = 0.6V \), \( V_{CC} = 22.5V \), and \( R_C = 5.6 \) K is used as shown in Fig.2. It is desired to establish a Q point at \( V_{CE} = 12V \), \( I_C = 1.5 \) mA, and a stability factor \( S \leq 3 \). Find \( R_E \), \( R_I \), \( R_2 \).

OR

(a)' Derive the expression for Stability factor “S” (self- bias), the variation of \( I_C \) with respect to \( \beta \) in terms of \( S_2 \), keeping \( I_C \) and \( V_{BE} \) constant. (6)

(b) Prove that the stability factor \( S \) for the emitter-feedback bias circuit shown in Fig.3 is
\[ S = \frac{1 + \beta}{1 + \beta R_E / (R_B + R_E)} \]

Q3. (a) For the circuit shown in Fig. 4, the NMOS transistor has \( |V_i| = 0.9V \) and \( V_A = 50V \) and operates with \( V_D = 2V \). What is the voltage gain \( \frac{v_o}{v_i} \)? What do \( V_D \) and the gain become if \( I \) is increased to 1mA? (4)

(b) The transistor in the circuit shown in Fig.5 is biased to operate in the active mode. Assuming that \( \beta \) is very large, find the collector bias current \( I_C \). Replace the transistor with the small-signal equivalent circuit model. Analyze the resulting amplifier circuit to show that

Contd.....2.
\[
\frac{v_{01}}{v_i} = \frac{R_E}{R_E + r_e} \\
\frac{v_{02}}{v_{01}} = \frac{\alpha R_C}{R_E + r_e}
\]

Find the values of voltage gain (for \( \alpha = 1 \)). Now, if the labeled voltage \( v_{01} \) is connected to ground, what does the voltage gain \( \frac{v_{02}}{v_i} \) become?

Given that: \( R_C = 4.3k\Omega, R_E = 6.8k\Omega, R_{B1} = R_{B2} = 100k\Omega \).

**OR**

3' (a) Draw the small signal equivalent circuit for the common base amplifier. Calculate its voltage gain and short circuit current gain.

(b) A common-gate amplifier using an n-channel enhancement MOS transistor for which \( g_m = 5 \text{ mA/V} \) has a 5-k\( \Omega \) drain resistance (\( R_D \)) and a 2-k\( \Omega \) load resistance (\( R_L \)). The amplifier is driven by a voltage source having a 200-\( \Omega \) resistance. What is the input resistance of the amplifier? What is the overall voltage gain \( G_u \). If the circuit allows a bias-current increase by a factor of 4 while maintaining linear operation, what do the input resistance and the voltage gain become?

**Q4.** (a) Define and derive the expression for MOSFET unity gain frequency \( (f_t) \) taking high frequency model.

(b) Determine the overall low-frequency transfer function and all the break (corner) frequencies due to \( C_{C1}, C_{C2} \) and \( C_S \) in a common source amplifier.

**OR**

(b)' Find the mid-band gain and the upper 3-dB frequency of the common-emitter amplifier shown in Fig. 6.

Given: \( V_{CC} = V_{EE} = 10V, I = 1mA, R_B = 100K\Omega, R_C = 8K\Omega, R_{sig} = 5K\Omega, R_L = 5K\Omega, \beta_0 = 100, V_A = 100V, C_{mu} = 1pF, f_T = 800MHz \) and \( r_x = 50\Omega \).

**Q5.** (a) Define piezoelectric effect of crystal oscillator. Determine its series resonance and parallel resonance frequencies.

(b) Determine the input and output impedances of

(i) Current shunt feedback

(ii) Voltage series feedback

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\( Contd......3. \)